



# FSC-BT1104QI

DATASHEET V1.0

## 1 INTRODUCTION

### Overview

The FSC-BT1104QI module supports both Classic Bluetooth and LE Audio protocols.

It comes preloaded with Feasycom's robust and fully encapsulated firmware, designed for ease of integration. The firmware enables Bluetooth functionality to be accessed via straightforward ASCII commands over a serial interface, effectively functioning as a Bluetooth modem.

With its streamlined interface and powerful capabilities, the FSC-BT1104QI module offers an efficient and reliable solution for developers seeking to incorporate Bluetooth wireless technology into their applications with minimal development effort.

### Features

- Qualified to Bluetooth v5.4 specification
- 240 MHz audio DSP
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible LED controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I<sup>2</sup>C/SPI), USB 2.0
- 1 x unidirectional 16/24/32-bit inter-integrated circuit sound (I<sup>2</sup>S) interface
- Quad analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs
- Advanced audio algorithms Qualcomm® aptX™ and aptX HD Audio, AAC and LDAC
- aptX Adaptive, enabled using license key
- Class 1 Bluetooth power level supported

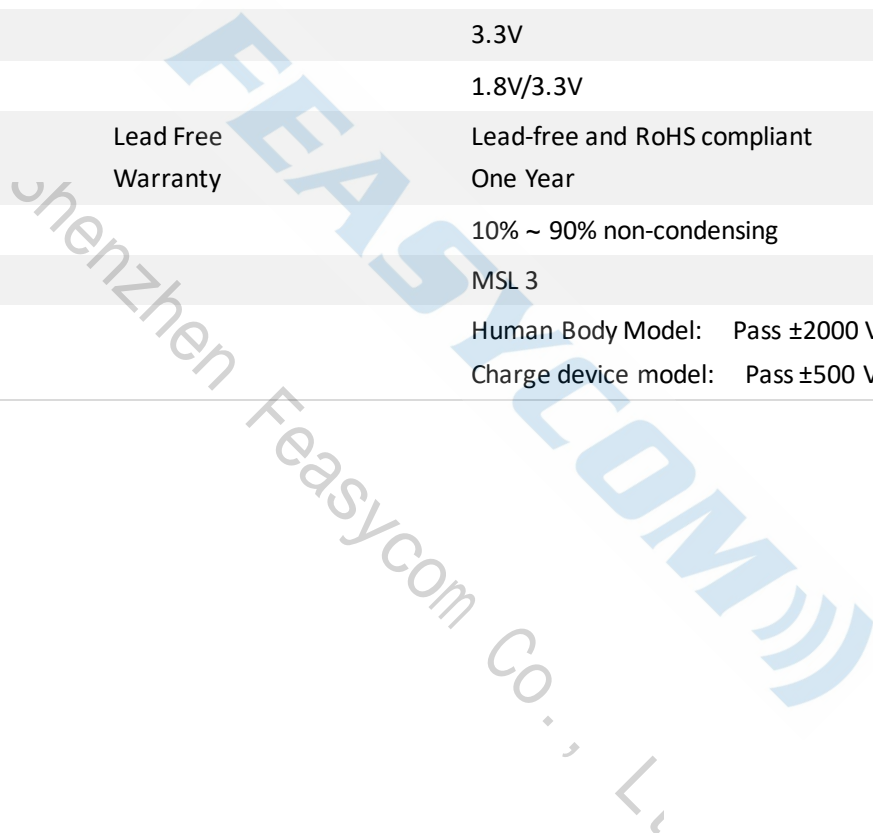
### Application

- Wireless speakers
- Wired/wireless stereo headsets/headphones

## 2 General Specification

Table 2-1: General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth v5.4
	Frequency Band	2402MHz~2480MHz
	Transmit Power	10 dBm
	Receiver	-93dBm
	Interface	UART/I <sup>2</sup> S/USB
Size		12 mm × 17 mm × 2.2mm
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Supply Voltage		3.3V
VDD_IO		1.8V/3.3V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V
		Charge device model: Pass ±500 V





## 3.2 Module Package Type

LGA package, as shown in the figure below.

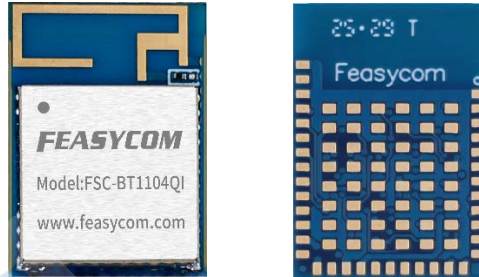


Figure 3-2: FSC-BT1104QI Package Module Appearance

## 3.3 PIN Definition Descriptions

Table 3-2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	SYS_CTRL	I	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull.	
3	MIC_LP	I	Microphone 1 differential input, positive/ Differential audio line input 1, positive	
4	MIC_LN	I	Microphone 1 differential input, negative./ Differential audio line input 1, negative	
5	MIC_RN	I	Microphone 2 differential input, negative./ Differential audio line input 2, negative	
6	MIC_RP	I	Microphone 2 differential input, positive./ Differential audio line input 2, positive	
7	MIC_BIAS	O	Mic bias output.	
8	SPK_LP	O	Differential line output 1, positive	
9	SPK_LN	O	Differential line output 1, negative	
10	VDD_IO	I	IO VDD 1.8V/3.3V	
11	PIO34/I2C_SDA	I/O	Programmable I/O Alternative function: I2C_SDA	
12	PIO35/I2C_SCL	I/O	Programmable I/O Alternative function: I2C_SCL	

13	SPK_RN	O	Differential line output 2, negative
14	SPK_RP	O	Differential line output 2, positive
15	PIO18/I2S_DOUT	I/O	Programmable I/O Alternative function: I2S_DOUT
16	PIO16/I2S_BCLK	I/O	Programmable I/O Alternative function: I2S_BCLK
17	PIO19/I2S_DIN	I/O	Programmable I/O Alternative function: I2S_DIN
18	PIO17/I2S_WS	I/O	Programmable I/O Alternative function: I2S_WS
19	PIO15/I2S_MCLK	I/O	Programmable I/O Alternative function: I2S_MCLK
20	VDD	Vdd	3V3
21	GND	Vss	Power Ground
22	AIO0/LED0	I/O	General-purpose analog/digital input or open drain LED output.
23	AIO1/LED1	I/O	General-purpose analog/digital input or open drain LED output.
24	RESET	I	RESET
25	VBUS	I	USB Power
26	GND	Vss	Power Ground
27	USB_DP		USB Full Speed device D+
28	USB_DN		USB Full Speed device D-
29	PIO7	I/O	Programmable I/O line/ TBR_MISO[0]
30	PIO6	I/O	Programmable I/O line/ TBR_MOSI[0]
31	PIO8	I/O	Programmable I/O line/ TBR_CLK
32	PIO5/UART_TXD	I/O	Programmable I/O Alternative function:UART_TXD
33	PIO4/UART_RXD	I/O	Programmable I/O Alternative function:UART_RXD
34	PIO3/UART_CTS	I/O	Programmable I/O Alternative function:UART_CTS
35	GND	Vss	Power Ground
36	ANT	RF	Bluetooth transmit/receive.
37	GND	Vss	Power Ground
38	PIO45	I/O	Programmable I/O
39	VDD_USB/3V3_OUT	O	3.3V voltage output (MAX. 50mA OUT)
40	LINE3/MIC3_N	I	Microphone 3 differential input, negative.

			Alternative function: Differential audio line 3 input right, negative Microphone 3 differential input, positive.
41	LINE3/MIC3_P	I	Alternative function: Differential audio line 3 input right, positive
42	PIO2/UART_RTS	I/O	Programmable I/O Alternative function: UART_RTS
43	PIO50	I/O	Programmable I/O
44	PIO22	I/O	Programmable I/O
45	PIO53	I/O	Programmable I/O
46	PIO49	I/O	Programmable I/O
47	PIO41	I/O	Programmable I/O
			Microphone 4 differential input, positive.
48	LINE4/MIC4_P	I	Alternative function: Differential audio line 4 input right, positive Microphone 4 differential input, negative.
49	LINE4/MIC4_N	I	Alternative function: Differential audio line 4 input right, negative
50	PIO51	I/O	Programmable I/O
51	PIO37	I/O	Programmable I/O
52	PIO23	I/O	Programmable I/O
53	PIO52	I/O	Programmable I/O
54	PIO39	I/O	Programmable I/O
55	PIO42	I/O	Programmable I/O
56	PIO44	I/O	Programmable I/O
57	PIO40	I/O	Programmable I/O
58	PIO36	I/O	Programmable I/O
59	PIO47	I/O	Programmable I/O
60	PIO48	I/O	Programmable I/O
61	PIO25	I/O	Programmable I/O
62	AIO2/LED2	I/O	General-purpose analog/digital input or open drain LED output.
63	PIO29	I/O	Programmable I/O
64	PIO21	I/O	Programmable I/O
65	PIO43	I/O	Programmable I/O
66	PIO27	I/O	Programmable I/O
67	NC		

68	AIO4/LED4	I/O	General-purpose analog/digital input or open drain LED output.
69	PIO24	I/O	Programmable I/O
70	PIO38	I/O	Programmable I/O
71	PIO31	I/O	Programmable I/O
72	PIO28	I/O	Programmable I/O
73	PIO32	I/O	Programmable I/O
74	CHG_EXT	O	External charger transistor current control.
75	AIO3/LED3	I/O	General-purpose analog/digital input or open drain LED output.
76	AIO5/LED5	I/O	General-purpose analog/digital input or open drain LED output.
77	PIO46	I/O	Programmable I/O
78	VDD_PADS_356	I	IO VDD 1.8V/3.3V
79	PIO20	I/O	Programmable I/O
80	PIO26	I/O	Programmable I/O
81	PIO30	I/O	Programmable I/O
82	1V8_SMPS	O	1.8V voltage output
83	PIO33	I/O	Programmable I/O
84	VCHG_SENSE	I	Charger input sense pin after external mode sense-resistor. High impedance. NOTE: If using internal charger connect VCHG_SENSE direct to VCHG.
85	VBAT_SENSE	I	

## 4 PHYSICAL INTERFACE

### 4.1 UART Interface

The FSC-BT1104QI module features a standard 4-wire UART interface, including RX, TX, CTS, and RTS signals. It supports both H4 HCI interface and raw UART communication to the application. The default baud rate is set to 115.2 kbps. To accommodate various communication speeds, the FSC-BT1104QI offers multiple UART clock options, enabling flexibility for high and low-speed data transfer.

The UART signal levels are compatible with a range from 1.8V to 3.3V. The host provides the necessary power supply to the UART interface through the VIO\_HOST pin, ensuring the appropriate voltage level for stable operation.

Table 4-1: Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 1200 baud (18.62%Error)
	Standard 115200bps(0.03%Error)
	Maximum 4Mbps(0%Error)
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

### 4.2 Standard I<sup>2</sup>S/PCM Interface

FSC-BT1104QI provides a standard I<sup>2</sup>S/PCM interface capable of operating at up to a 384 kHz sample rate.

The I<sup>2</sup>S/PCM port is highly configurable with alternate PCM modes, and has the following options:

- SYNC edge position selectable to align with start of channel data (PCM mode), or 1 clock before start of channel data (I<sup>2</sup>S mode)
- Master (generate CLK and SYNC) or Slave (receive CLK and SYNC) (PCM/I<sup>2</sup>S)
- SYNC polarity (PCM)
- Long or short SYNC (PCM)
- Left or right justification (PCM/I<sup>2</sup>S)
- Sign extension / zero pad (PCM)
- Optional tri-state at end of word (PCM)
- Optional invert of clock (PCM/ I<sup>2</sup>S)
- 13/16/24-bit per sample (PCM/ I<sup>2</sup>S)
- Up to four slots per frame (PCM)

Table 4-2: PCM and I<sup>2</sup>S pin and signal names

I <sup>2</sup> S Pin	PCM function	Description
I <sup>2</sup> S_SD_IN/SDIN/ADCDAT	PCM_IN	Data input
I <sup>2</sup> S_WS/FS/LRCLK	PCM_SYNC	Word sync

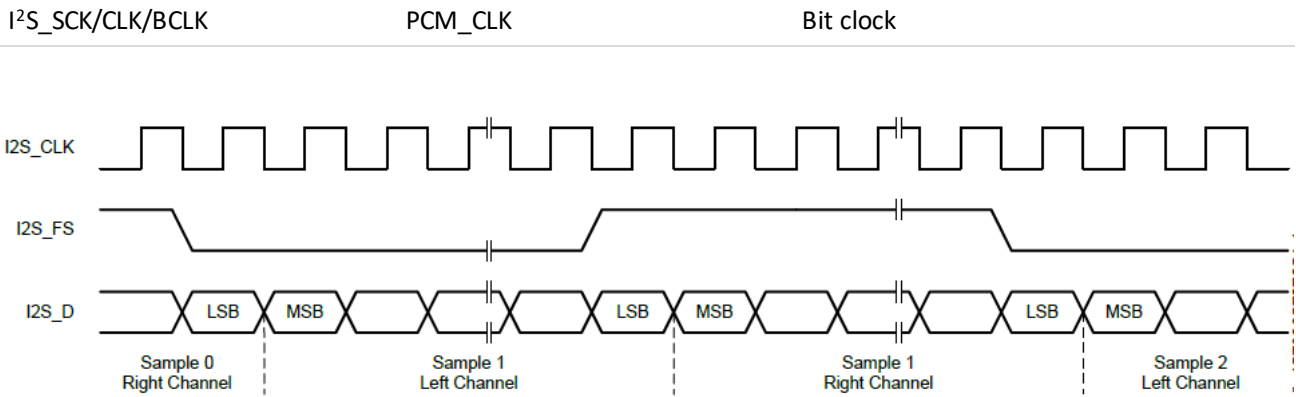


Figure 4-2: I²S general format

### 4.2.1 I²S/PCM master mode timing diagram

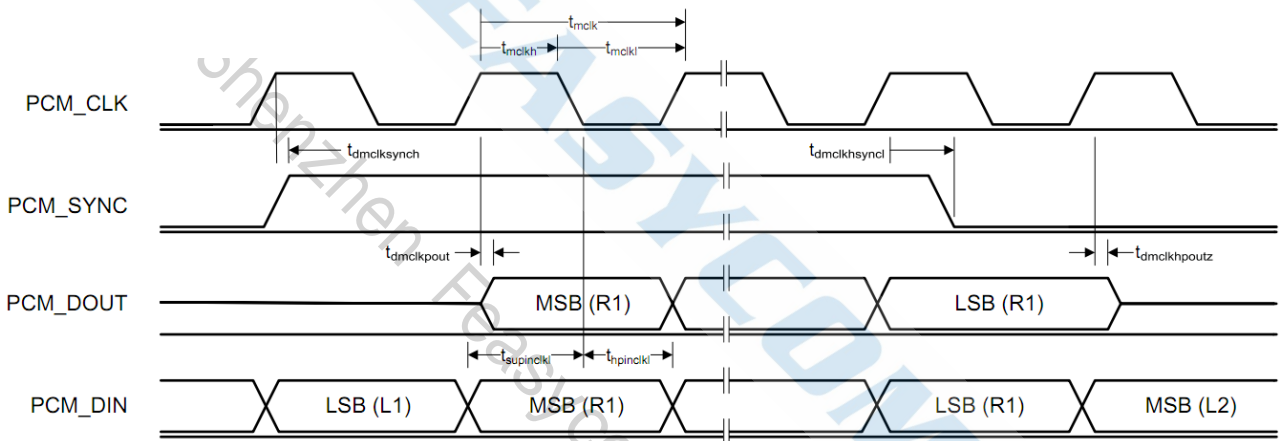


Figure 4-2-1: I²S/PCM master mode timing diagram

**NOTE**

- Diagram shows I²S standard format, but timing information also applies to PCM mode.
- PCM\_DOUT to tri-state is not applicable in I²S mode, because I²S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- $1/t_{mclk}$  is the audio sample frequency. I²S specification requires that  $t_{mclkh}$  and  $t_{mckl}$  must be greater than or equal to  $0.35 t_{mclk}$

Table 4-2-1: I²S/PCM master mode timing diagram symbols

Parameter	Min	Type	Max	Unit
$t_{dmclksynch}$ - Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$ - Delaytime from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclksyncl}$ - Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$T_{dmclhpoutz}$ - Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinckl}$ - Set-up time for PCM_IN valid to PCM_CLK low	-	-	20	ns

$t_{hpincclk}$ - Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	ns
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### 4.2.2 I<sup>2</sup>S/PCM slave mode timing diagram

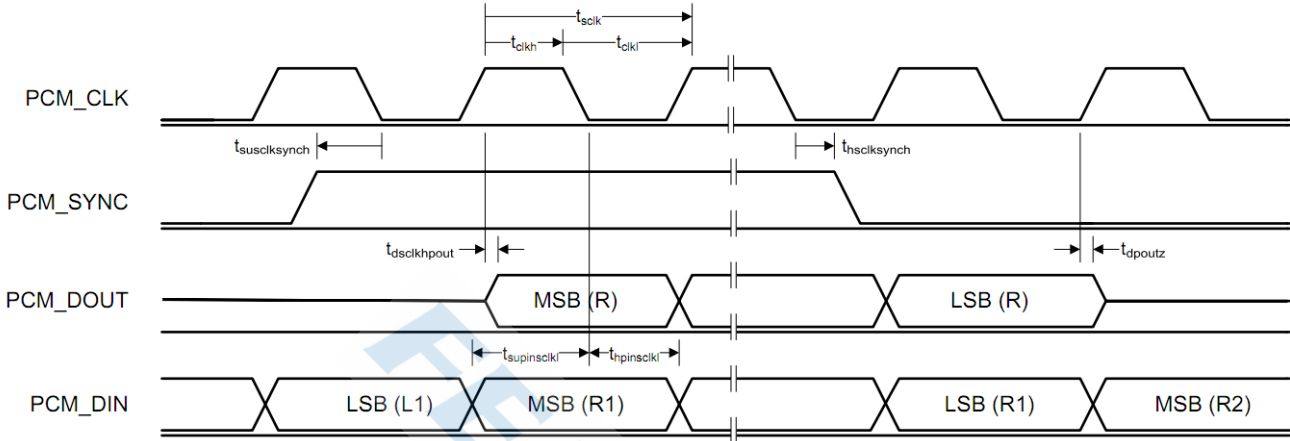


Figure 4-2-2: I<sup>2</sup>S/PCM slave mode timing diagram

**NOTE**

- Diagram shows I<sup>2</sup>S standard format, but timing information also applies to PCM mode.
- PCM\_DOUT to tri-state is not applicable in I<sup>2</sup>S mode, because I<sup>2</sup>S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- $1/t_{sckl}$  is the audio sample frequency. I<sup>2</sup>S specification requires that  $t_{sclkh}$  and  $t_{sckl}$  must be greater than or equal to  $0.35 t_{sckl}$

Table 4-22: I<sup>2</sup>S/PCM slave mode timing diagram symbols

Parameter	Min	Type	Max	Unit
$t_{hscclksynch}$ - Hold time from PCM_CLK low to PCM_SYNC high	5	-	-	ns
$t_{usclksynch}$ - Set-up time for PCM_SYNC high to PCM_CLK low	15	-	-	ns
$t_{dscclhpout}$ - Delay time from PCM_CLK high to PCM_OUT valid data	-	-	20	ns
$t_{dpoutz}$ - Delay time from PCM_CLK high to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsckl}$ - Set-up time for PCM_IN valid to PCM_CLK low	15	-	-	ns
$t_{hpinsckl}$ - Hold time for PCM_CLK low to PCM_IN invalid	5	-	-	ns

## 4.3 Analog audio Interfaces

### 4.3.1 Line/mic input

FSC-BT1104QI has two high-quality audio input ADCs (HQADC), primarily intended for line input use, but also suitable for other applications that support mixed differential and single ended use cases. The ADC is 24-bit, and

capable of sample rates from 8 kHz to 96 kHz. The HQADC is configurable, with an internal switch arrangement, see

Figure 9. VAG is a virtual ground reference. The software API allows for direct control of the nine switches, or a simpler control, supporting three standard modes:

- Stereo differential input
- Stereo single ended input, using the P inputs
- Stereo single ended input, using the N inputs

Inputs should be AC coupled, typically with a 2u2 capacitor. This capacitor value can be reduced at the expense of low frequency response attenuation.

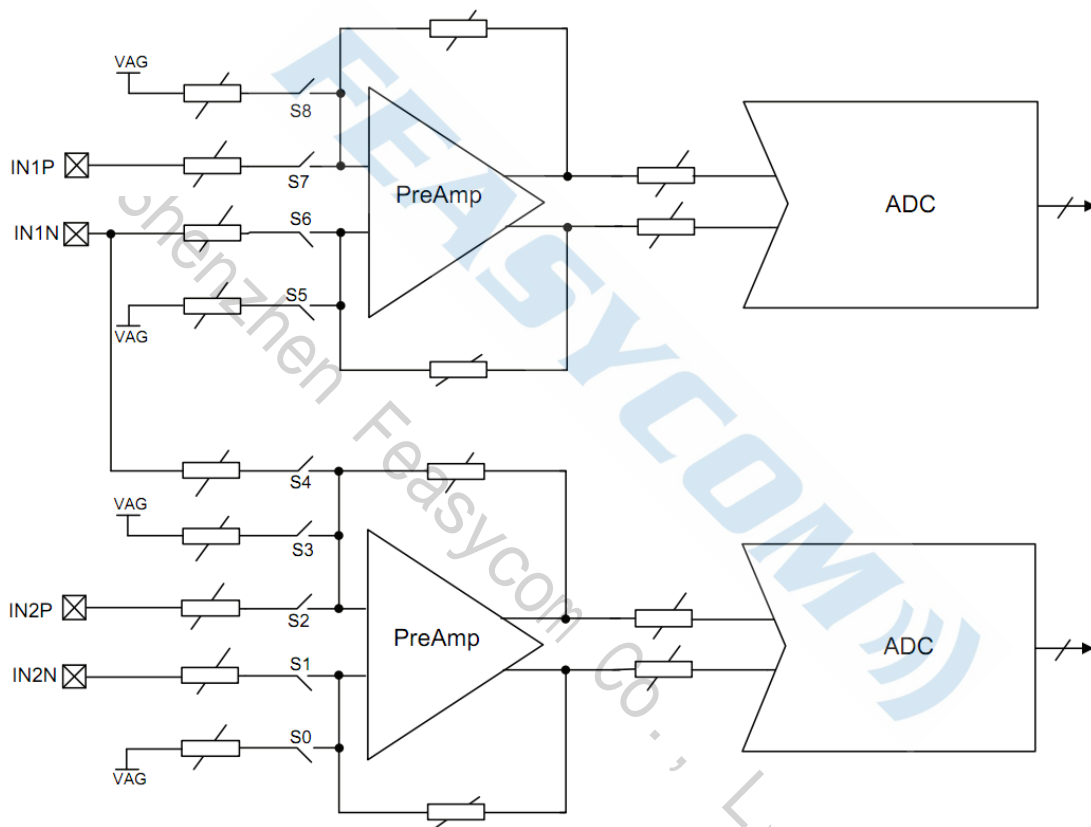


Figure 4-3-1: high-quality ADC input switch configuration

#### 4.4 USB Interfaces

- FSC-BT1104QI has a USB device interface: An upstream port, for connection to a host Phone/PC
- The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically FSC-BT1104QI enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.
- The DP 1.5 k pull-up is integrated in FSC-BT1104QI. No series resistors are required on the USB data lines.
- FSC-BT1104QI contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.

- Extra ESD protection is not required on VCHG (VBUS) because FSC-BT1104QI meets the USB certification requirements of a minimum of 1 $\mu$ F, and a maximum of 10  $\mu$ F being present on VCHG (VBUS).
- The VCHG input of FSC-BT1104QI is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.
- FSC-BT1104QI supports charger detection to the USB BCv1.2 standard.
- Updater and RF testing

## 4.5 Programming and Debug Interfaces

FSC-BT1104QI provides a debug (Pin27\29\30) interface for programming, updata, configuring, and debugging the FSC-BT1104QI.

## 4.6 Standard PIO

The standard digital I/O pins (PIO) on FSC-BT1104QI are split into separate pad domains. Each VDD\_IO domain can be separately powered, from 1.7 V to 3.3 V. When PIOs in a supply domain are used for a high-speed interface, decoupling the respective VDD\_IO pin with a 100 nF decoupling capacitor may be beneficial. The VDD\_IO of a particular pin should be powered before voltages are applied to any PIO powered by that domain, otherwise back powering can occur through the electrostatic discharge (ESD) protection in the pad.

PIO can be programmed to have a pull-up or pull down with two strengths (weak and strong). PIO can also be programmed with a sticky function where they are strongly pulled to their current input state. PIO have a reset pull state, after reset the pulls can be re-configured by software.

PIO also have a programmable drive strength capability of 2, 4, 8, or 12 mA.

All PIO are readable by all subsystems, but for write access are assigned by software to particular subsystem control. PIO inputs are via Schmitt triggers.

## 4.7 SYS\_CTRL pin

- SYS\_CTRL is an input pin that acts as a power on signal for the internal regulators.
- From the OFF state, SYS\_CTRL must be asserted for >2s to start power up.
- SYS\_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS\_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.
- Use software to logically disconnect SYS\_CTRL from the power on signal for internal regulators. For example, when booted, software takes control of the internal regulators and the state of SYS\_CTRL is ignored by the regulators.

## 4.8 Reset pin

FSC-BT1104QI is digital reset pin (RESET#) is an active low reset signal.

The pin is active low and on-chip glitch filtering avoids the need to filter out any spurious noise that may cause unintended resets. The RESET# pin has a fixed strong pull-up to VDD\_IO, and therefore can be left unconnected. The input is asynchronous, and is pulse extended within FSC-BT1104QI to ensure a full reset

FSC-BT1104QI contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after unintended reset (such as a severe ESD event). Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down if VCHG is not present and SYS\_CTRL is low. FSC-BT1104QI then requires a SYS\_CTRL assertion or VCHG attach to restart.

#### NOTE

- FSC-BT1104QI is always powered if VCHG is present. It does not power down if RESET# is asserted while VCHG remains present.
- FSC-BT1104QI is powered down via software-controlled methods rather than external assertion of RESET#.
- Holding RESET# low continuously is not the lowest FSC-BT1104QI power state, because pull downs are enabled on VCHG and VDD\_USB in this state.
- RESET# is guaranteed to work if held low for 120  $\mu$ s

## 4.9 LED Drivers

- LED Driver: This mode is designed for driving LEDs. The pad operates as an open-drain pad, tolerable of voltages up to 7.0 V. Therefore the cathode of the LED should be connected to the FSC-BT1104QI LED pad. Each pad is rated to sink up to 50 mA of current.
- FSC-BT1104QI has five PWM-based LED controllers controlled by the Applications subsystem. Use them for driving either the LED pads (through virtual PIOs) or other available PIOs.
- An application may configure the LED flash rate and ramp time using a dedicated API.
- Once configured, the LED flash and ramp rate are fully hardware controlled within the LED/PWM module. It is possible to synchronize any number of the LED drivers together. Use the flash/ramp rate configuration to generate color change sequences on RGB LEDs.

## 5 ELECTRICAL CHARACTERISTICS

### 5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)

Table 5-1: Absolute Maximum Rating

Parameter	Min	Type	Max	Unit
VCHG	-0.4		6.5	V
VBAT	-0.4		4.8	V
VDD_IO	-0.4		3.8	V
Digital I/O	-0.4		3.8	
LED/AIO	-0.4		+7/2.1	V
MIC_BIAS	-0.4		2.1	V
Storage temperature (T <sub>stg</sub> )	-40		85	°C

### 5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VCHG	4.75	5.0	5.5	V
VBAT	3.0	3.3	4.2	V
VDD_IO	1.8	3.3	3.6	V
Digital I/O	0	3.3	3.6	
LED/AIO	0		6.5/1.95	V
MIC_BIAS	1.7		1.95	V
Operating temperature (T <sub>A</sub> )	-40		85	°C

## 6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

## 7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccant (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

**Note:** The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccant and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

*Notice:*

*Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.*

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

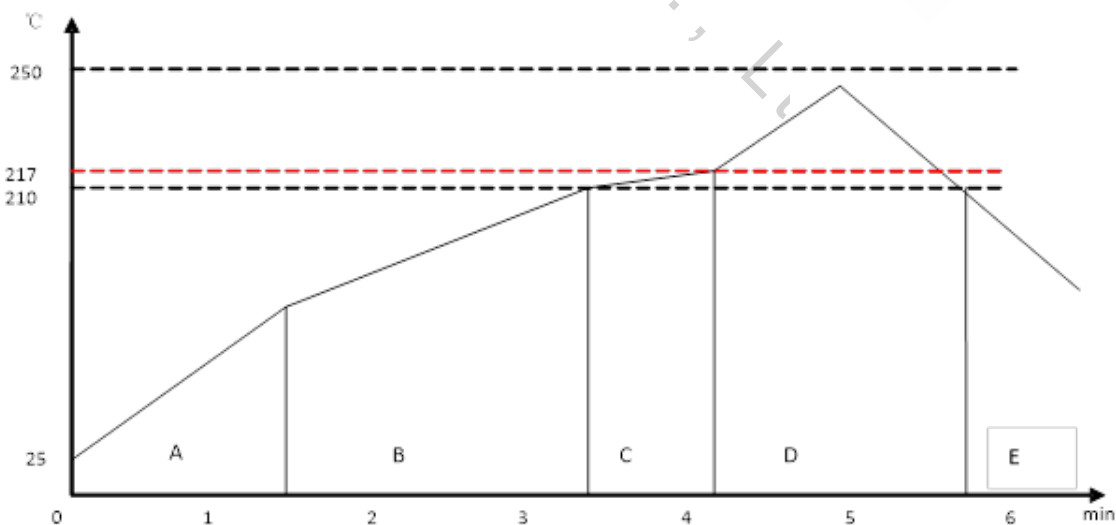


Figure 7-1: Typical Lead-free Re-flow

**Pre-heat zone (A)** — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

**Equilibrium Zone 1 (B)** — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

**Equilibrium Zone 2 (C) (optional)** — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

**Reflow Zone (D)** — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

**Cooling Zone (E)** — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

## 8 MECHANICAL DETAILS

### 8.1 Mechanical Details

- Dimension: 12mm(W) x 17mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 12mm X 17mm Tolerance: ±0.2mm
- Pad size: 0.8mmX0.5/0.6mm Tolerance: ±0.2mm
- Pad pitch: 0.9/1.2mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

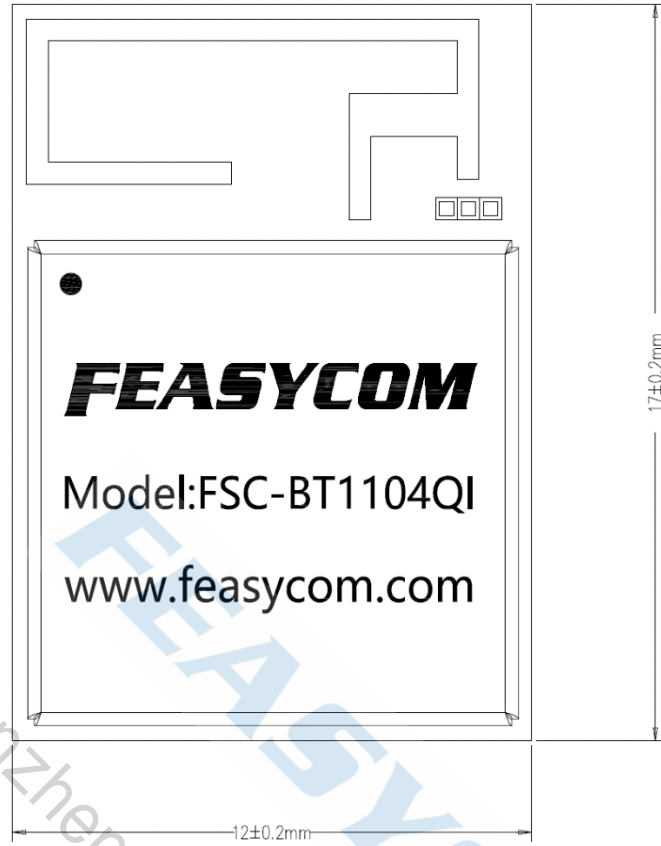


Figure 8-1: FSC-BT1104QI footprint Layout Guide (Top View)

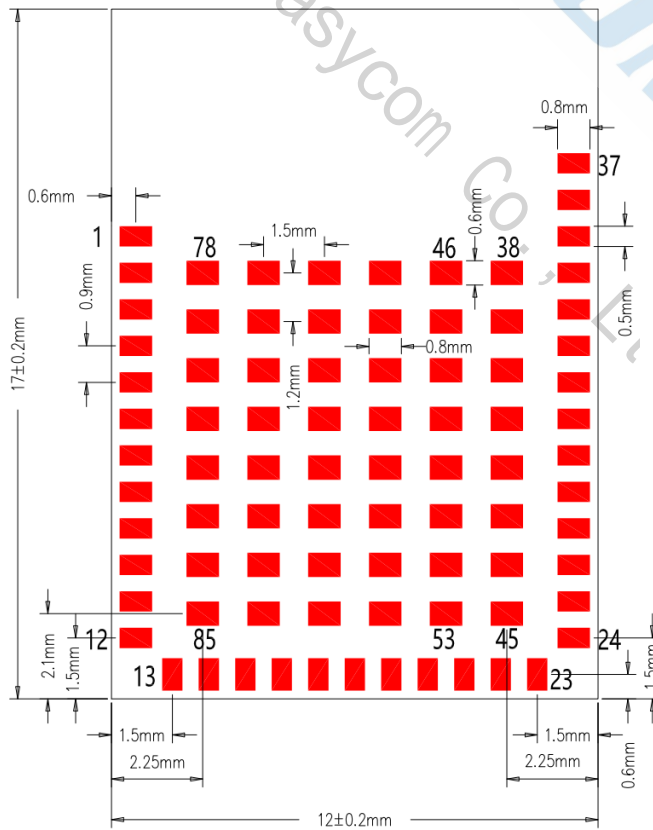


Figure 8-2: FSC-BT1104QI footprint Layout Guide (Top View)

## 9 HARDWARE INTEGRATION SUGGESTIONS

### 9.1 Soldering Recommendations

FSC-BT1104QI is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

### 9.2 Layout Recommendations for Product Design Structure

The onboard antenna of this module is a specially designed antenna. Its optimal performance characteristics are highly dependent on the actual product's structure, materials, module placement, the shape of the baseboard, and even the thickness and dimensions of the baseboard. Therefore, the customer's baseboard design must strictly adhere to this guide to achieve the best RF performance and complete real-world distance testing and validation.

#### 9.2.1 Module Layout Recommendations

**Recommendation 1:** Place the module in the middle of the main board (**the customer's baseboard must be hollowed out**). The TOP layer layout is shown in Figure 8-2-1:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

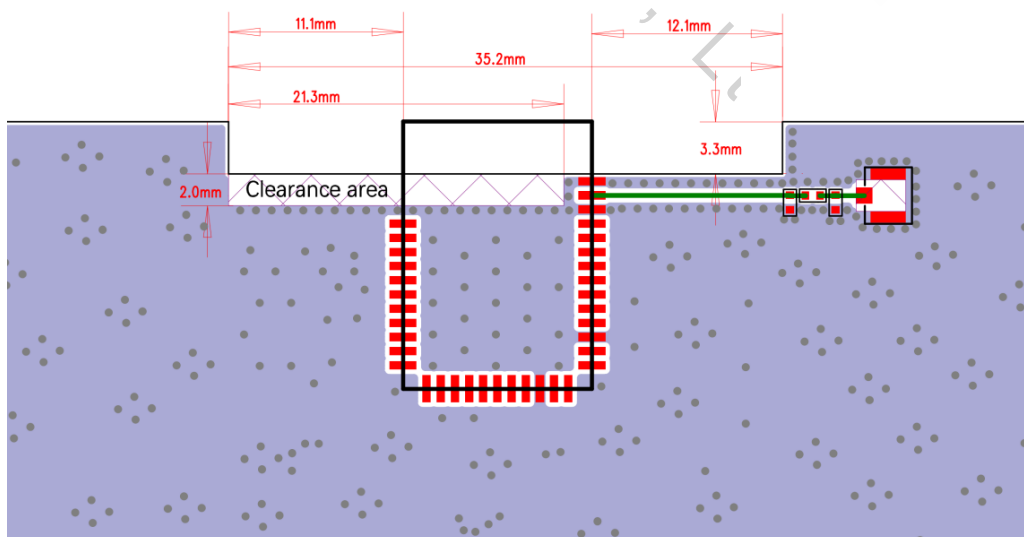


Figure 8-2-1: Module Layout - Baseboard TOP Layer

When the module is placed in the middle of the baseboard, the L2/L3/Ln...../Bottom layer layout is shown in Figure 8-2-2:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.3x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

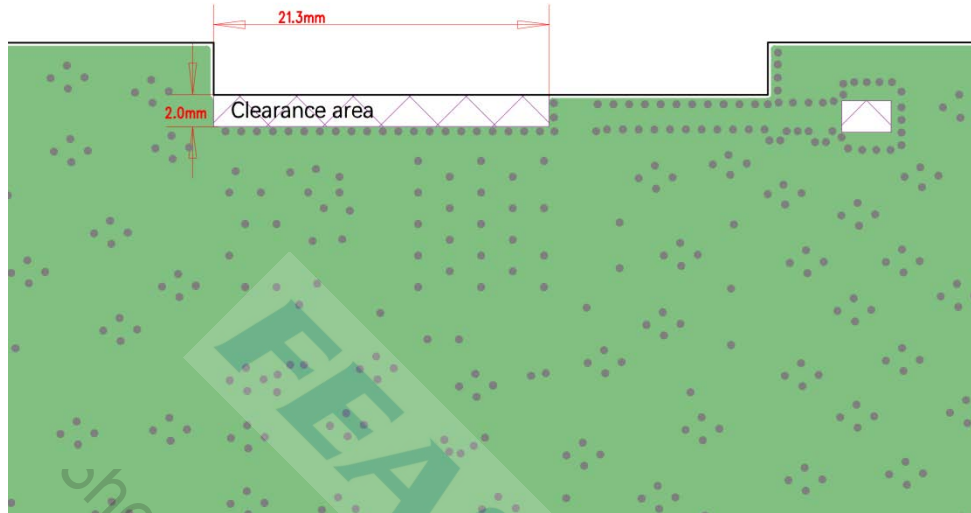


Figure 8-2-2: Module Layout - Baseboard L2/L3/BOTTOM Layers

**Recommendation 2:** Similar to Recommendation 1, place the module at the edge of the baseboard (**the customer's baseboard must be hollowed out**). The TOP layer layout is shown in Figure 8-2-3:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

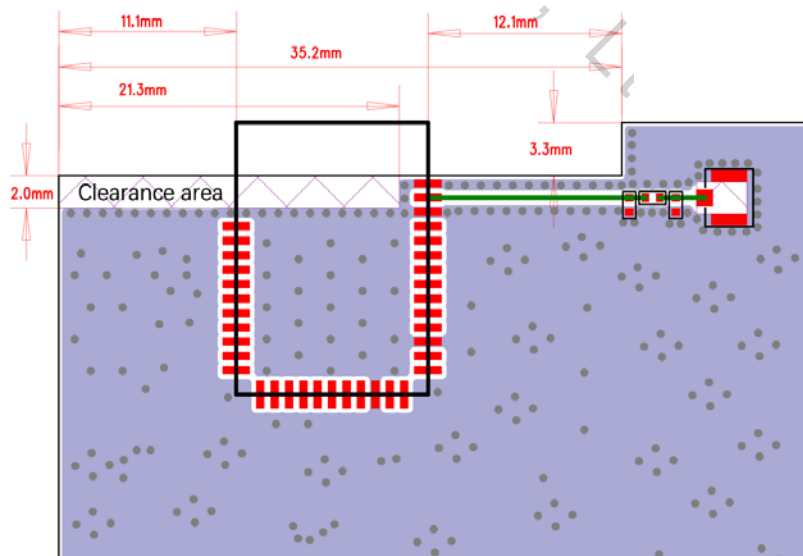


Figure 8-2-3: Module Layout - Baseboard TOP Layer

When the module is placed at the corner of the main board, the L2/L3/Ln...../Bottom layer layout is shown in Figure 8-2-4:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.23x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

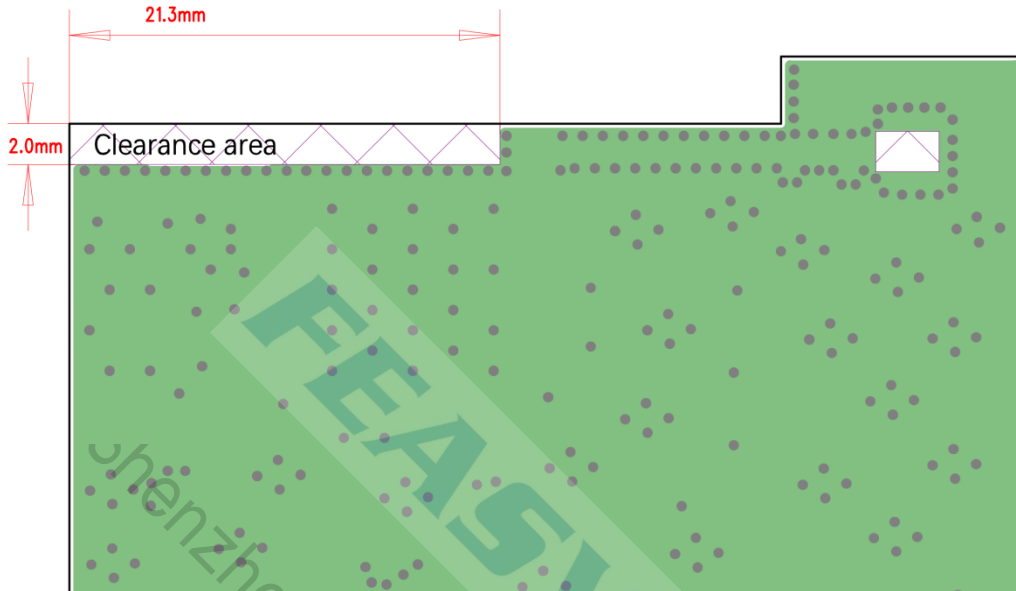


Figure 8-2-4: Module Layout - Main Board L2/L3/Ln...../BOTTOM Layers

### 9.2.2 Special Trace Recommendations

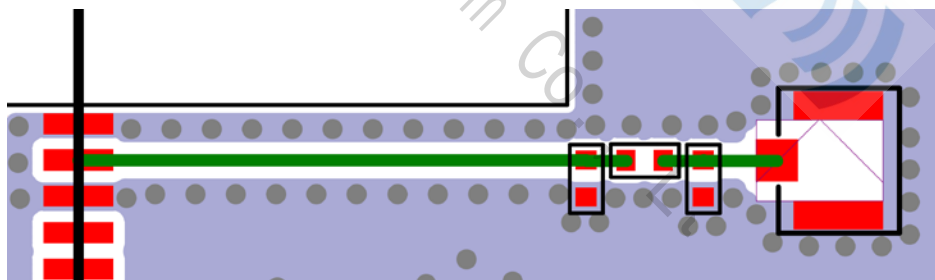


Figure 8-2-5: External Antenna Trace Schematic

The signal transmission line from the module to the antenna matching circuit should be a 50-ohm characteristic impedance microstrip line. The width of the microstrip line and the spacing from the ground copper must be determined based on the specific PCB layer stack-up. No intersecting lines are allowed between the microstrip line and the ground. All layers beneath the IPEX connector must be cleared (as shown by the purple cross-hatched area under the connector).

### 9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

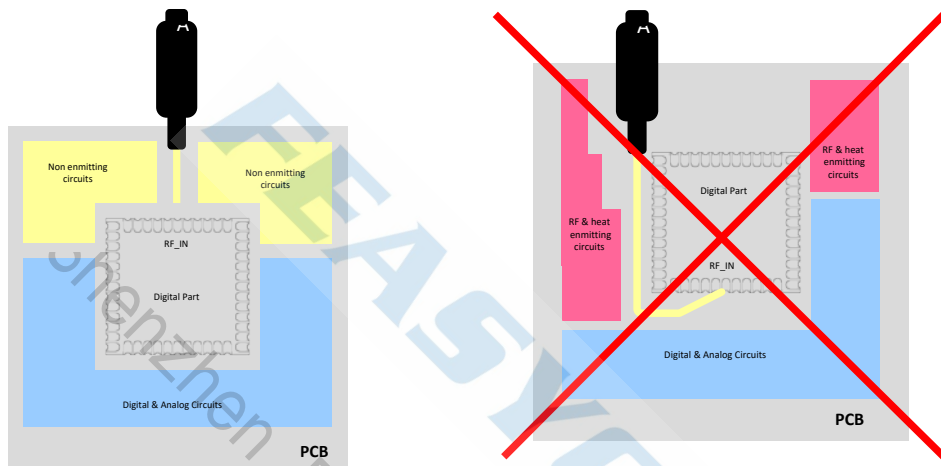


Figure 9-2: Placement the Module on a System Board

#### 9.3.1 Antenna Connection and Grounding Plane Design

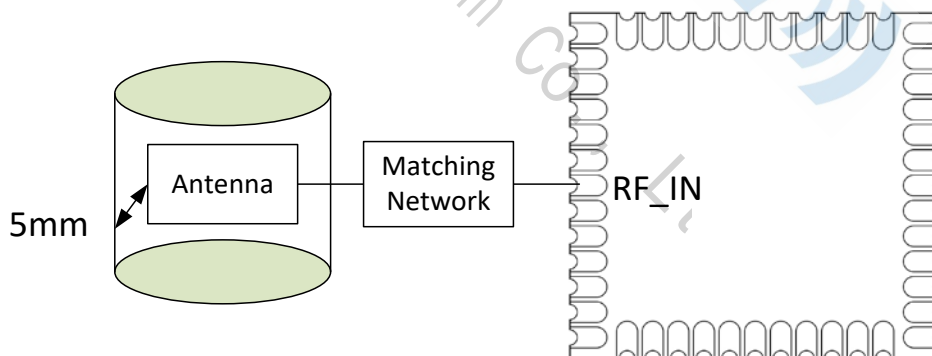


Figure 9-21-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

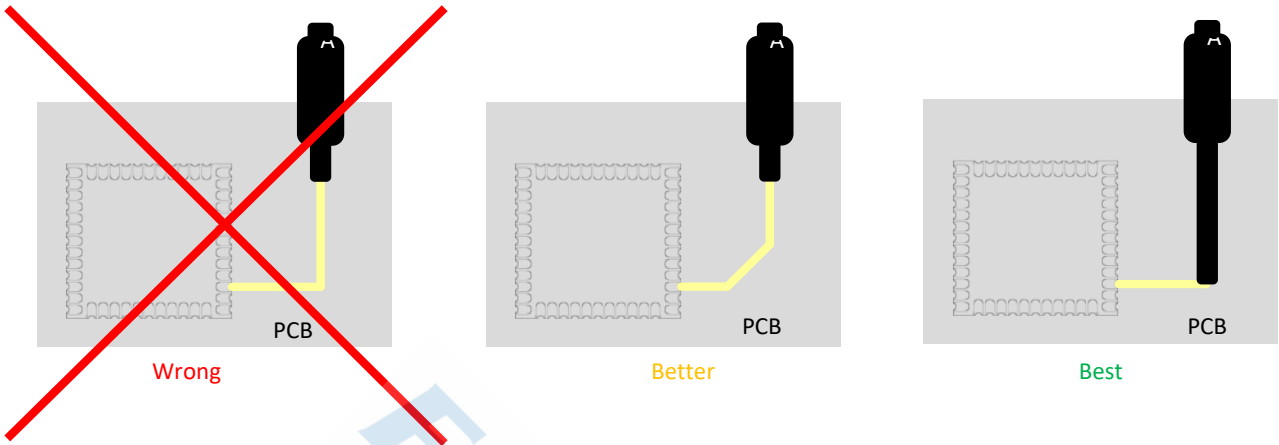


Figure 9-21-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

## 10 PRODUCT PACKAGING INFORMATION

### 10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 230mm \* 180mm\* 8mm



Figure 9-1: Tray vacuum

## 10.2 Packing box(Optional)

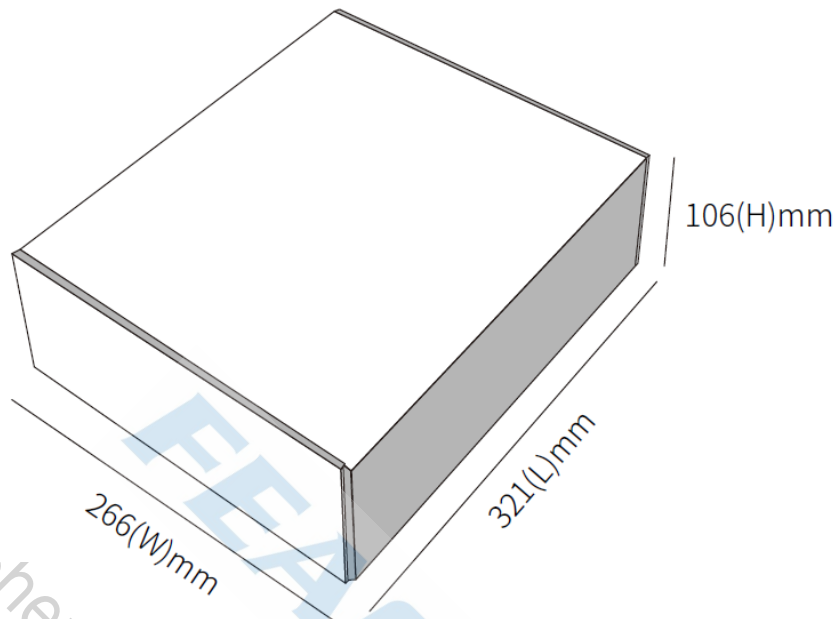


Figure 9-2: Packing box(Optional)

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*\* If other packing is required, please confirm with the customer*

*\* Packing: 1000pcs per carton (Minimum packing quantity)*

*\* The outer packing size is for reference only, please refer to the actual size*

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# APPLICATION SCHEMATIC

