FSC-BT1114QI

DATASHEET V1.0

Revision History

Version	Data	Notes	Writer
1.0	2025/04/15	Initial Version	Mo

Contact Us

Shenzhen Feasycom Co.,Ltd

Email: sales01@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District, Shenzhen, 518102, China
Tel: 86-755-27924639, 86-755-23062695

1 INTRODUCTION

Overview

FSC-BT1114QI supports Classic Bluetooth and LE Audio.

By default, the FSC-BT1114QI module comes with Feasycom's powerful and user-friendly firmware, which is fully encapsulated and easy to use. This firmware allows users to access Bluetooth functionality through simple ASCII commands sent over a serial interface, functioning much like a Bluetooth modem.

As a result, the FSC-BT1114QI is an ideal solution for developers looking to integrate Bluetooth wireless technology into their designs.

Features

- Qualified to Bluetooth v5.4 specification
- 240 MHz audio DSP
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible LED controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I^2C/SPI), USB 2.0
- 1 x unidirectional 24-bit inter-integrated circuit sound (I^2S) interface
- Sony/Philips digital interface (SPDIF): Two instances configurable as inputs
- Quad analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs
- Class 1 Bluetooth power level supported
- PCB antenna

Application

- USB dongles and source devices

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth	Chip	QCC3086
	Bluetooth Standard	Bluetooth v5.4
	Frequency Band	2402MHz~2480MHz
	Transmit Power	10 dBm
	Receiver	-93dBm
	Interface	UART/I²S/USB
Size		12mm × 17 mm × 2.2mm
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Supply Voltage		3.0V~4.6V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V Charge device model: Pass ±500 V

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

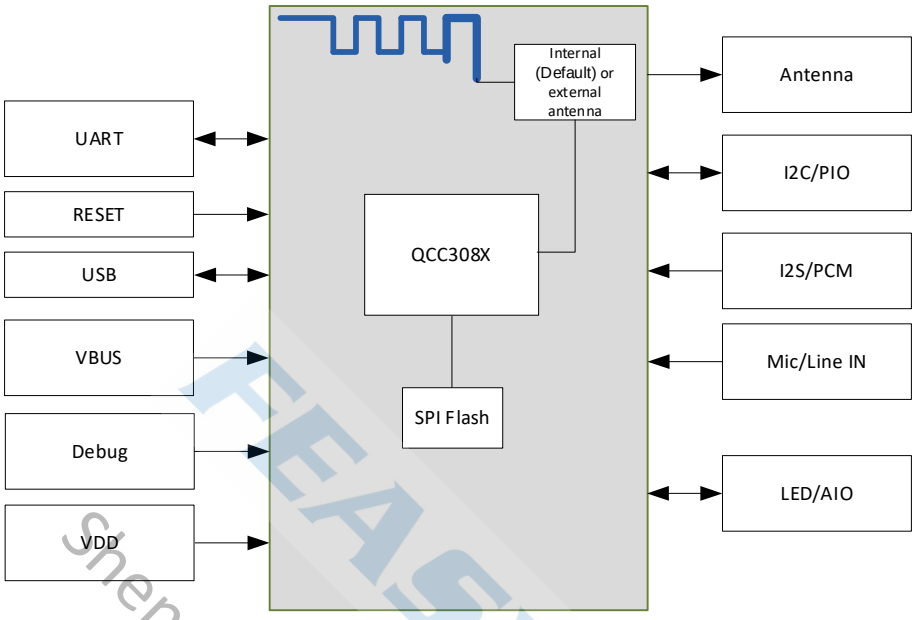

Figure 3-1:Block Diagram

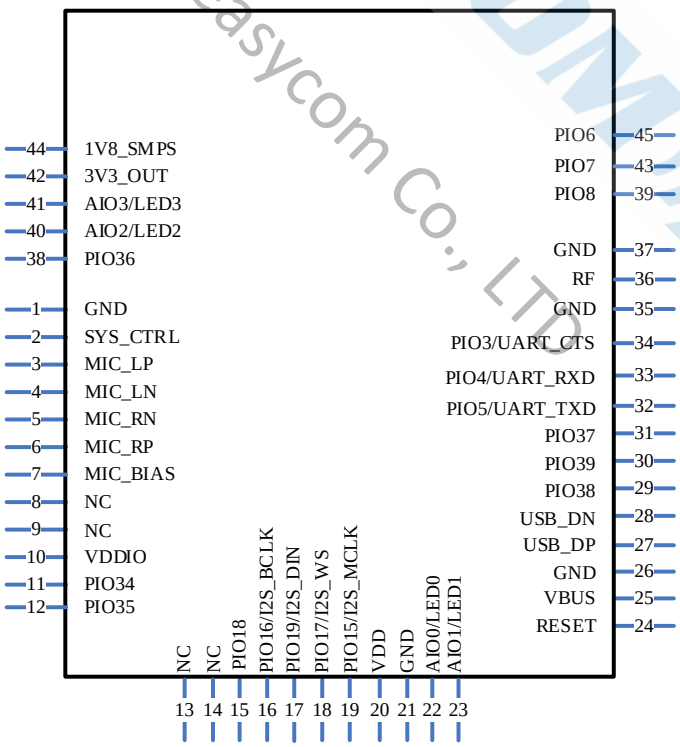

Figure 3-2:FSC-BT1114QI PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 3-2：Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	SYS_CTRL	I	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull.	
3	MIC_LP	I/O	Microphone differential 1 input, positive/ Differential audio line input 1, positive	
4	MIC_LN	I/O	Microphone differential 1 input, negative./ Differential audio line input 1, negative	
5	MIC_RN	I/O	Microphone differential 2 input, negative./ Differential audio line input 2, negative	
6	MIC_RP	I/O	Microphone differential 2 input, positive./ Differential audio line input 2, positive	
7	MIC_BIAS	I/O	Mic bias output	
8	NC			
9	NC			
10	VDD_IO	Supply	1.8V/3.3V	
11	PIO34	I/O	Programmable I/O Alternative function: I2C_SDA	
12	PIO35	I/O	Programmable I/O Alternative function: I2C_SCL	
13	NC			
14	NC			
15	PIO18	I/O	Programmable I/O	
16	PIO16/I2S_BCLK	I/O	Programmable I/O Alternative function: I2S_BCLK	
17	PIO19/I2S_DIN	I/O	Programmable I/O Alternative function: I2S_DIN	
18	PIO17/I2S_WS	I/O	Programmable I/O Alternative function: I2S_WS	
19	PIO15/I2S_MCLK	I/O	Programmable I/O Alternative function: I2S_MCLK	
20	VDD	VDD	3V3	

21	GND	Vss	Power Ground
22	AIO0/LED0	I/O	General-purpose analog/digital input or open drain LED output
23	AIO1/LED1	I/O	General-purpose analog/digital input or open drain LED output
24	RESET	I	RESET
25	VBUS	I	USB Power(4.75~5.25V)
26	GND	Vss	Power Ground
27	USB_DP		USB Full Speed device D+
28	USB_DN		USB Full Speed device D-
29	PIO38	I/O	Programmable I/O
30	PIO39	I/O	Programmable I/O
31	PIO37	I/O	Programmable I/O
32	UART_TXD	I/O	Alternative function: UART_TXD
33	UART_RXD	I/O	Alternative function: UART_RXD
34	UART_CTS	I/O	Alternative function: UART_CTS
35	GND	Vss	Power Ground
36	RF	RF	Bluetooth transmit/receive
37	GND	Vss	Power Ground
38	PIO36	I/O	Programmable I/O
39	PIO8	I/O	Programmable I/O line/ TBR_CLK
40	AIO2/LED2	I/O	General-purpose analog/digital input or open drain LED output
41	AIO3/LED3	I/O	General-purpose analog/digital input or open drain LED output
42	3V3_OUT	O	3.3V/2.9V OUT
43	PIO7	I/O	Programmable I/O line/ TBR_MISO[0]
44	1V8_SMPS	O	1.8V OUT
45	PIO6	I/O	Programmable I/O line/ TBR_MOSI[0]

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT1114QI UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. It supports both the H4 HCI interface and raw UART for application use. The default baud rate is 115.2 k baud. To support both high and low baud rates, FSC-BT1114QI provides multiple UART clock options.

The UART signal level ranges from 1.8 V to 3.3 V. The host supplies the power to the UART interface at the appropriate voltage level via the VIO_HOST pin.

Table 4-1：Possible UART Settings

Parameter	Possible Values
Baud rate	Minimum 9600 baud (≤0%Error)
	Standard 115200bps(≤0.08%Error)
	Maximum 2Mbps(≤0%Error)
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5 MSL & ESD

Table 5-1: MSL and ESD

Parameter	Value
MSL grade	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute maximum ratings

Table 6-1：Absolute maximum ratings

Parameter	Pin	Min	Max	Unit
Storage Temperature	-	-40	85	°C
Supply voltage				
VCHG	VBUS	-0.4	6	V
Battery	VDD	-0.4	4.8	V
VDD IO	VDD_IO	-0.4	3.8	V
1.8 V	MIC_LN/ LINEIN_1_N MIC_LP/ LINEIN_1_P MIC_RN/ LINEIN_2_N MIC_RP/ LINEIN_2_P	-0.4	2.1	V
Digital I/O	PIO,RESET	-0.3	3.6	V
	VDD_IO	-0.3	3.6	V
	AIO/LED[1:0] (Disabled / Digital Input / Open Drain Output Modes)	0	4.8	V
	AIO/LED[1:0] (AIO Mode)	0	1.95	V
	SYS_CTRL	-0.4	4.8	V
All ground / VSS pads	-	-0.4	0.4	V
DC Voltage	BT_RF	0	0	V
Radio Receive	BT_RF	-0.4	0.4	V
Radio Transmit (3:1 VSWR)	BT_RF	-1.6	1.6	V

CAUTION: Stressing the device beyond the Absolute Maximum Ratings may cause instantaneous and permanent damage. Device performance is not guaranteed beyond the Recommended Operating Conditions. Prolonged exposure beyond the Recommended Operating Conditions may permanently affect device reliability and/or performance.

6.2 Recommended operating conditions

Table 6-2：Power Supply Characteristics

Parameter	Pin	Min	Typ	Max	Unit
Operating temperature range	-	-40	25	85	°C
Charger operating temperature range	-	-10	25	85	°C
Supply voltage					
5 V (USB VBUS)	VBUS	4.75	5.00	5.5	V
Battery	VDD	3.0 / 2.8(b)	3.7	4.6	V

	MIC_BIAS	0	-	2.3	V
	USB_DN	0	-	3.6	V
	USB_DP	0	-	3.6	V
1.8 V	MIC_LN / LINEIN_1_N MIC_LP/ LINEIN_1_P MIC_RN/ LINEIN_2_N MIC_RP / LINEIN_2_P	1.65	1.80	1.95	V
Digital I/O	VDD_IO	1.7	1.8	3.6	V
	PIO	0	-	VDD_IO	V
	RESET	0	-	3.5	V
	AIO/LED[1:0] (Disabled / Digital Input / Open Drain Output Modes)	0	-	5	V
	AIO/LED[1:0] (AIO Mode)	0	-	1.95	V
	SYS_CTRL	0	-	4.6	V
All ground / VSS pads	-	0	-	0	V

a：Minimum input voltage of 4.75 V is required for full specification.

b：Recommended software power-off threshold at 3.0 V. Device operates down to 2.8 V.

6.3 Digital terminals

Table 6-3：Digital terminals

Digital terminals	Min	Typ	Max	Unit
VDD_IO supply	1.7	1.8	3.6	V
VIL input logic level low	-	-	0.25 x VDD_IO	V
VIH input logic level high	0.625 x VDD_IO	-	-	V
Drive current (configurable)	2,4,8,12	4	-	mA
VOL output logic level low, at configured drive current	-	-	0.22 x VDD_IO	V
VOH output logic level high, at configured drive current	0.75 x VDD_IO	-	-	V
Strong pull (up and down)	50	70	125	kΩ
Weak pull (up and down)	729	1050	1350	kΩ

6.4 LED driver pins

Table 6-4：LED driver pads

Digital terminals		Min	Typ	Max	Unit
Open drain current	High impedance state	-	-	5	μA
	Current sink state	-	-	50	mA
LED pad resistance	V < 0.5 V	-	-	12	Ω
VIL input logic level low		-	-	0.4	V
VIH input logic level high		0.8	-	-	V

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice:

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modified with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

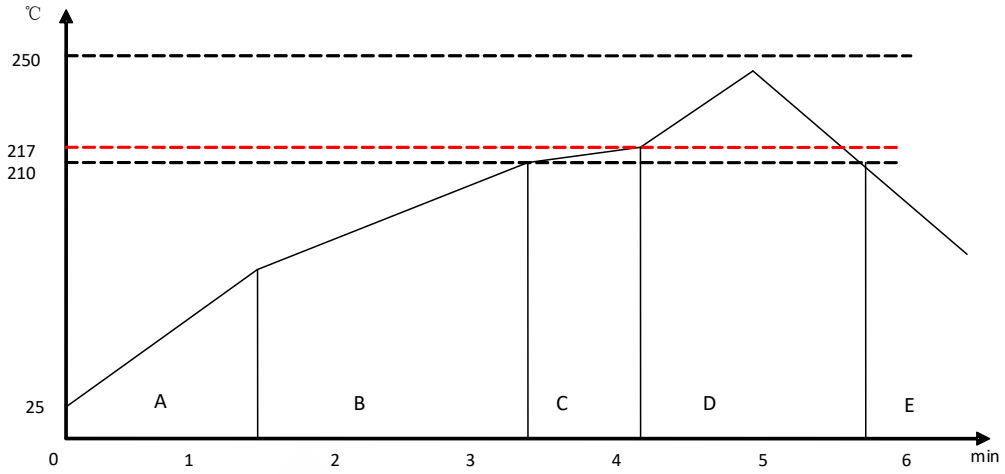

Figure 7-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. And it is also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 12mm(W) x 17mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 12mm X 17mm Tolerance: ±0.2mm
- Pad size: 1.7mmX0.5mm Tolerance: ±0.2mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

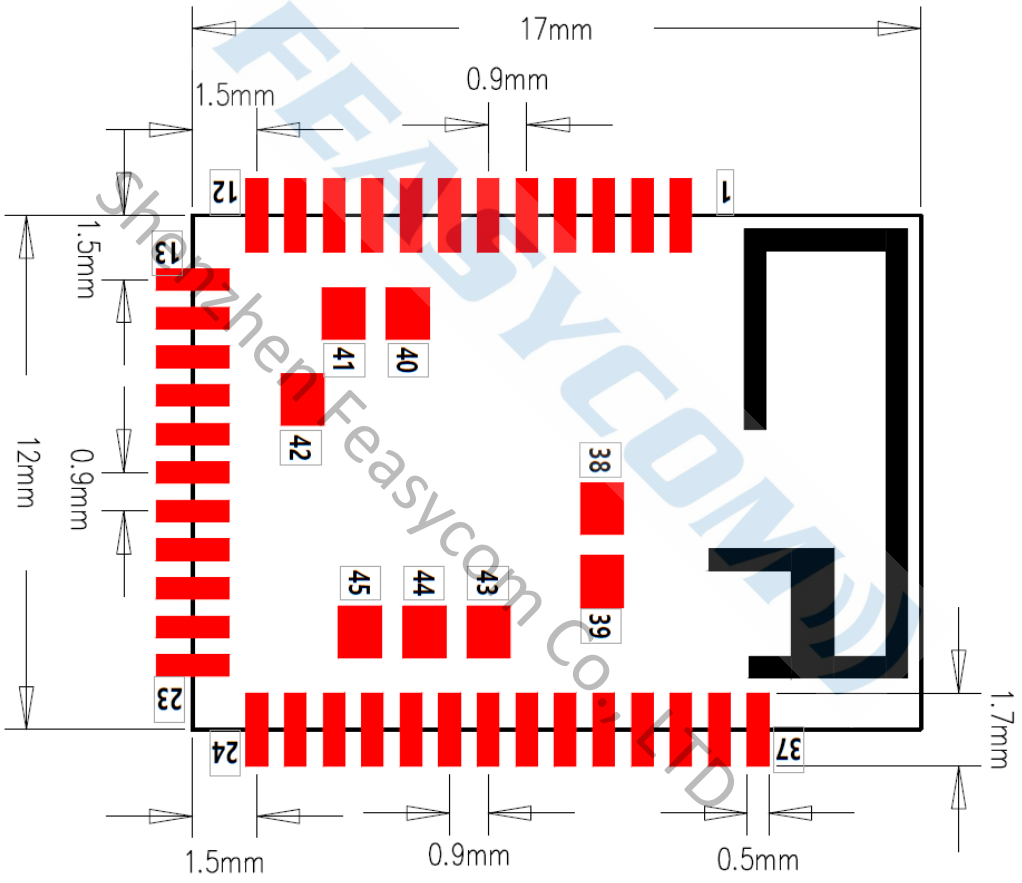

Figure 8-1: FSC-BT1114QI footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1114QI is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Recommendations for Product Design Structure

The onboard antenna of this module is a specially designed antenna. Its optimal performance characteristics are highly dependent on the actual product's structure, materials, module placement, the shape of the baseboard, and even the thickness and dimensions of the baseboard. Therefore, the customer's baseboard design must strictly adhere to this guide to achieve the best RF performance and complete real-world distance testing and validation.

9.2.1 Module Layout Recommendations

Recommendation 1: Place the module in the middle of the main board **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 9-2-1:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

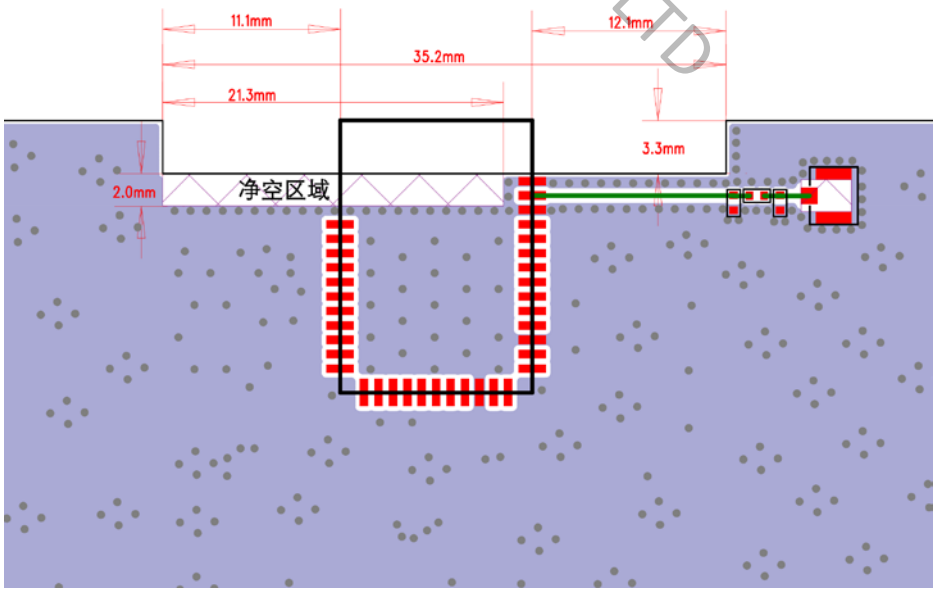

Figure 9-2-1： Module Layout - Baseboard TOP Layer

When the module is placed in the middle of the baseboard, the L2/L3/Ln...../Bottom layer layout is shown in Figure 9-2-2:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.3x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

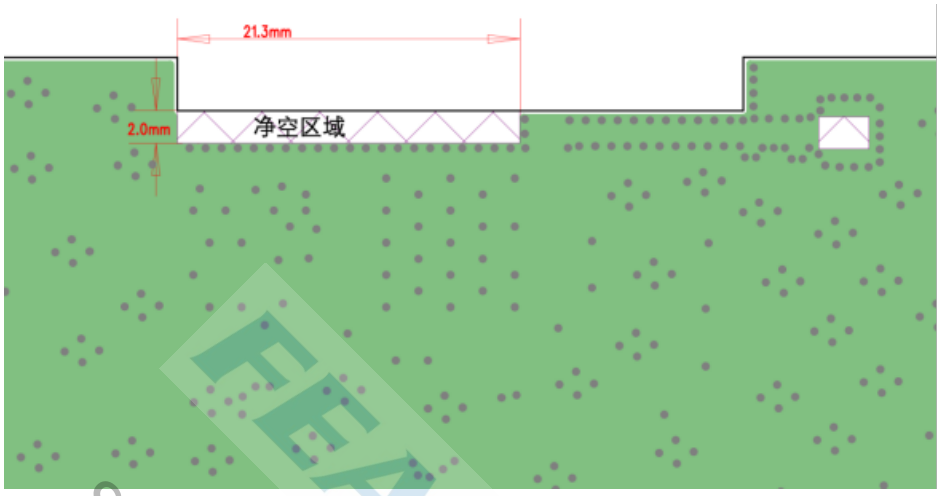

Figure 9-2-2： Module Layout - Baseboard L2/L3/BOTTOM Layers

Recommendation 2: Similar to Recommendation 1, place the module at the edge of the baseboard **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 9-2-3:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

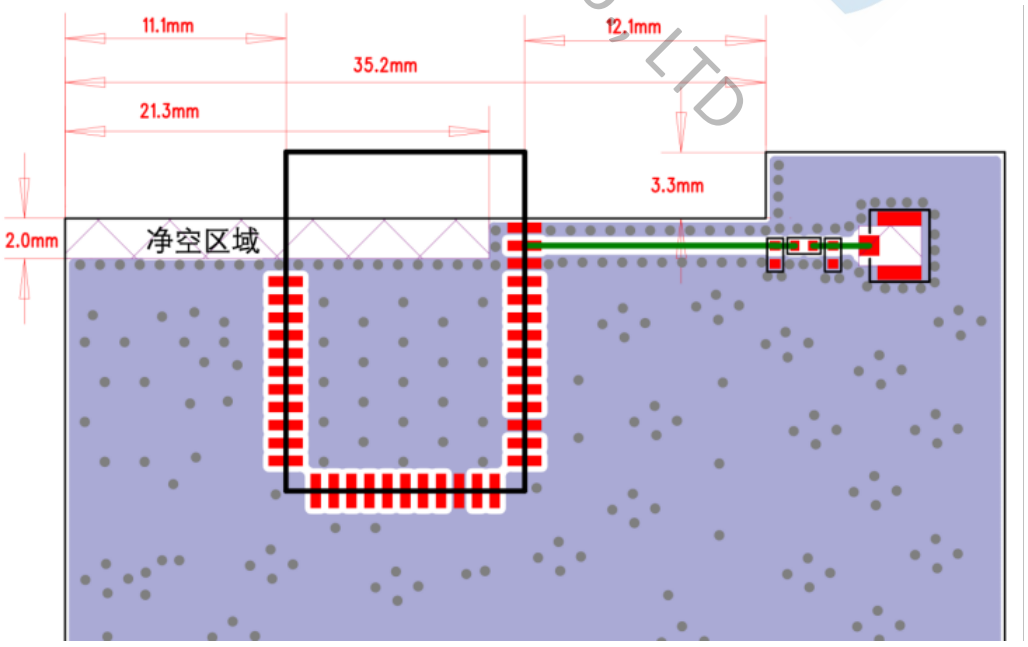

Figure 9-2-3： Module Layout - Baseboard TOP Layer

When the module is placed at the corner of the main board, the L2/L3/Ln...../Bottom layer layout is shown in Figure 9-2-4:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.23x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

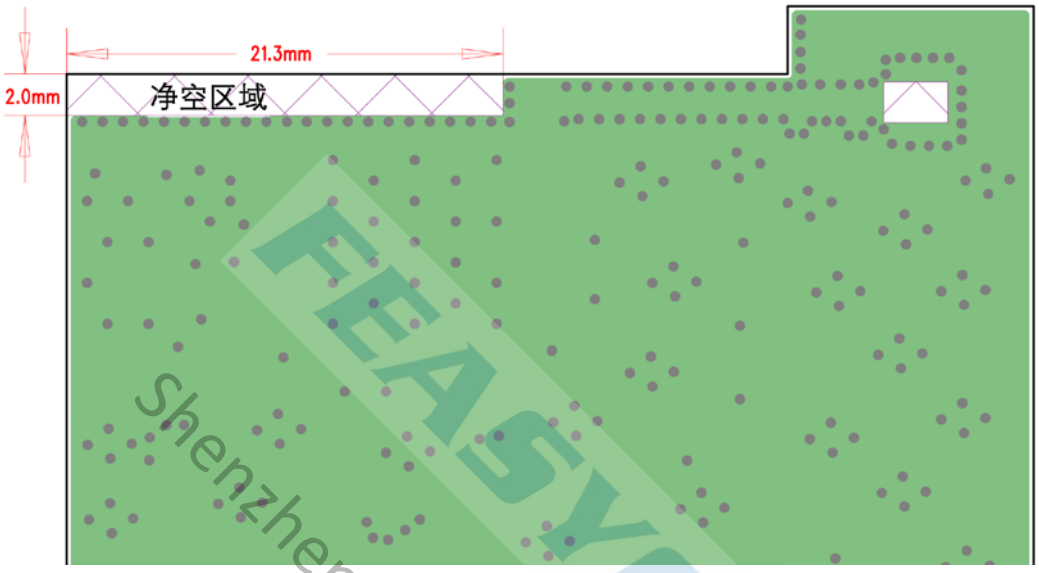

Figure 9-2-4： Module Layout - Main Board L2/L3/Ln...../BOTTOM Layers

9.2.2 Special Trace Recommendations

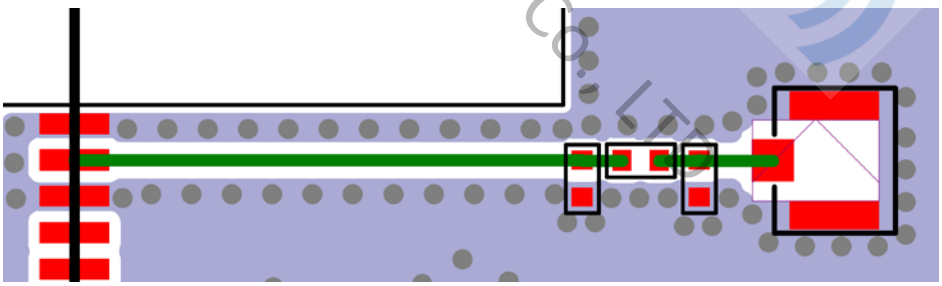

Figure 9-2-5： External Antenna Trace Schematic

The signal transmission line from the module to the antenna matching circuit should be a 50-ohm characteristic impedance microstrip line. The width of the microstrip line and the spacing from the ground copper must be determined based on the specific PCB layer stack-up. No intersecting lines are allowed between the microstrip line and the ground. All layers beneath the IPEX connector must be cleared (as shown by the purple cross-hatched area under the connector).

9.3 Layout Guidelines (External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

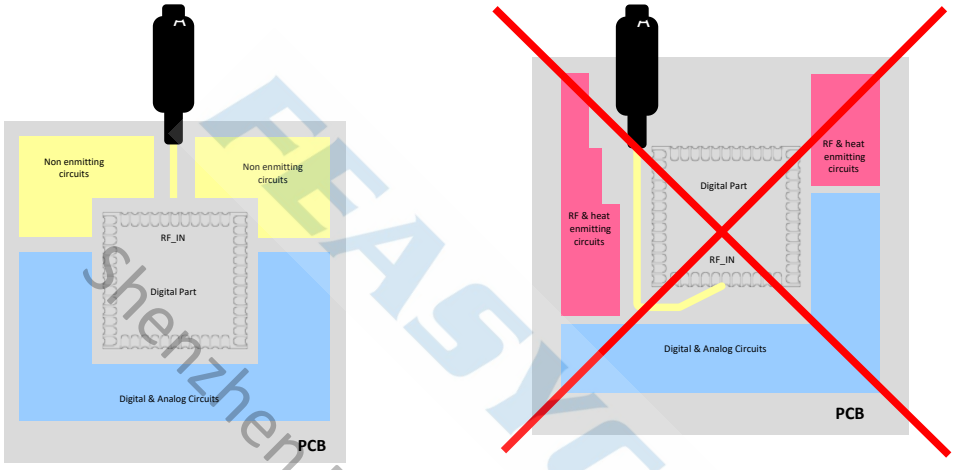

Figure 9-3-1: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

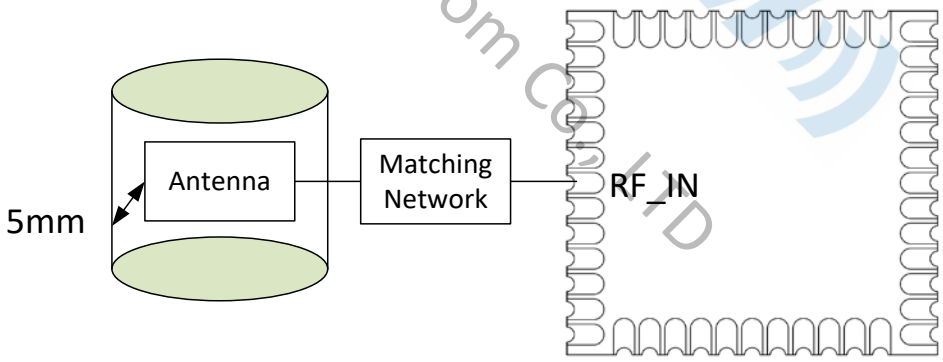

Figure 9-3-2: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

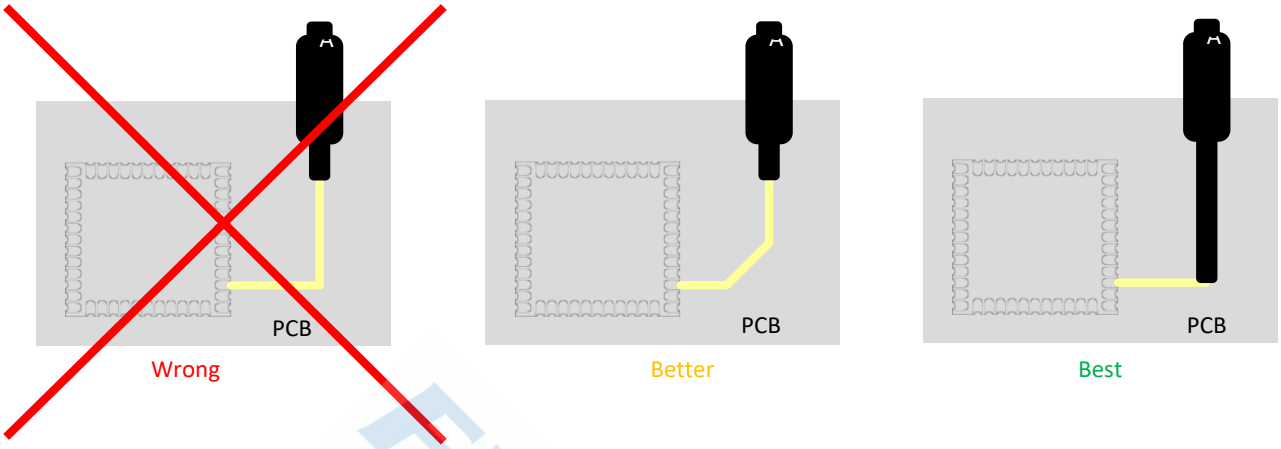

Figure 9-3-3: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 230mm * 180mm*8mm

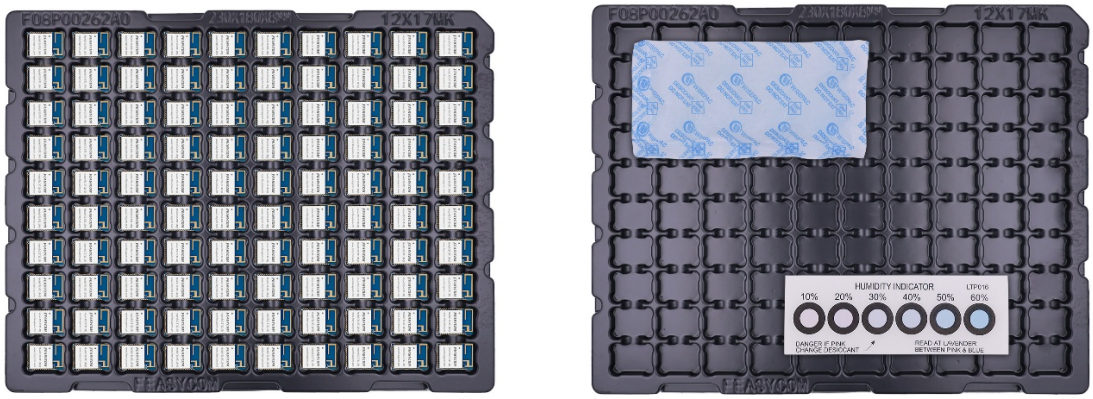

Figure 10-1: Tray vacuum

10.2 Packing Box (Optional)

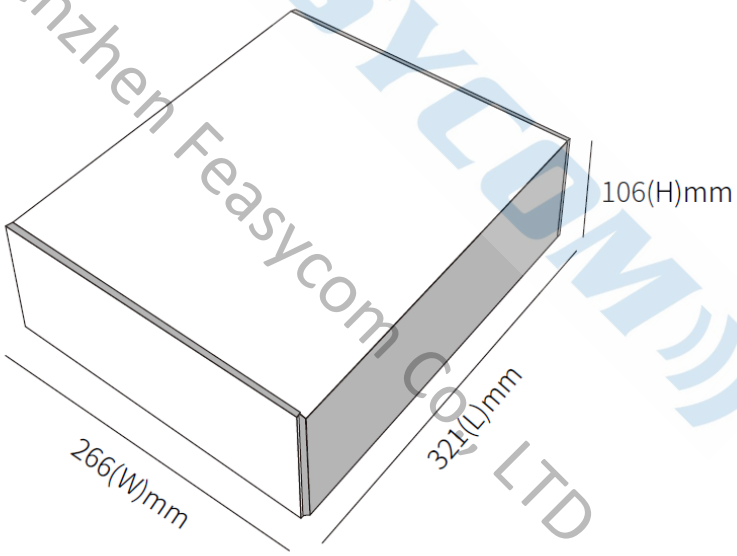

Figure 10-2: Packing box (Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

11 APPLICATION SCHEMATIC