FSC-BT2002RV

DATASHEET V1.1

Revision History

Version	Data	Notes	Author
V1.0	2025-07-23	Initial Version	Ma
V1.1	2025-08-31	The stamp holes of the module have been changed to LGA packaging.	Ma

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1 INTRODUCTION

Overview

The FSC-BT2002RV is a highly integrated module for BR/EDR/BLE. It allows one active link in either slave mode or master mode. For low energy consumption, it supports multiple states and allows an active link to be in slave mode. BR/EDR link and an LE link can be active at the same time.

The communication between Host and module is facilitated through UART port, and with FeasyBlue Bluetooth stack, users can control all Bluetooth audio and data transmission through simple API functions.

Therefore, FSC-BT2002RV provides an ideal solution for developers who wish to integrate Bluetooth wireless technology into their design.

The FSC-BT2002RV offers automotive Grade 2 (-40°C to +85°C) ambient operating temperature performance, while being AEC-Q100 Group A Grade 2 compliant.

Features

- **Bluetooth 5.3 specification compliant**
  - Bluetooth classic (BDR/EDR)
  - Bluetooth low energy (BLE)
    - Generic access service
    - Device information service
    - LE Isochronous Channel(CIS/BIS/ISOAL)
    - Support LE Audio CIS/BIS Auracast
- **High speed digital peripheral interfaces: UART**
- **Integrated 32K oscillator for power management**
- **Bluetooth Controller**
  - Compatible with Bluetooth v2.1 and v3.0 systems
  - Supports Bluetooth 5.3 Low Energy (BLE)
  - HS-UART interface for Bluetooth data transmission compliant with H4 specification
  - Integrates MCU to execute Bluetooth protocol stack
  - Supports all packet types in basic rate and enhanced data rate
  - Supports legacy pairing and secure simple pairing in BR/EDR and BLE
  - Supports Low Power Mode (Sniff mode)
  - Enhanced BT/Wi-Fi Coexistence Control to improve transmission quality in different profiles
  - Bluetooth 5.3 Dual Mode support simultaneous BLE and BR/EDR
  - Supports multiple Low Energy States

Applications

- Bluetooth KEY
- Smart home
- Data transmission module

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Chip Type		RTL8761CTV-VIQ-CG
Bluetooth	Bluetooth Standard	Bluetooth V5.3
	Frequency Band	2402MHz ~ 2480MHz
	Interface	UART/PCM/ I²S /I²C
	Transmit Power	+10 dBm (Max.)
	Receiver	-95dBm (Min.) @BLE 1Mbps
Profile		BLE/SPP/A2DP/HFP/AVRCP/PBAP/HICAR/AAP
Size		12mm(W) x 12mm(L) x 1.8mm(H) (without shielding cover) 12mm (W)× 12 mm (L)× 2.4mm(H) (with shielding cover)
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+105°C
Supply Voltage		3.3V（Typical）
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V, Charge Device Model: Pass ±500 V,

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

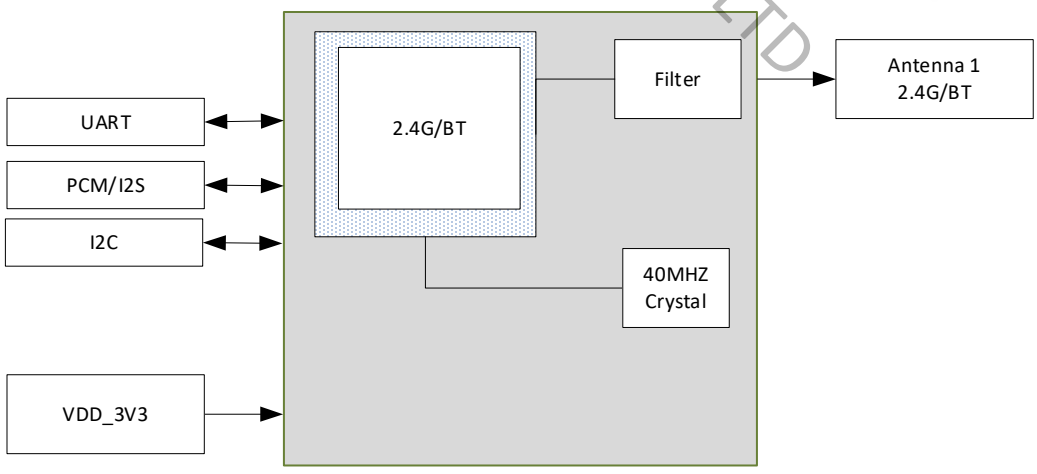


Figure 3-1-1: FSC-BT2002RV Block Diagram

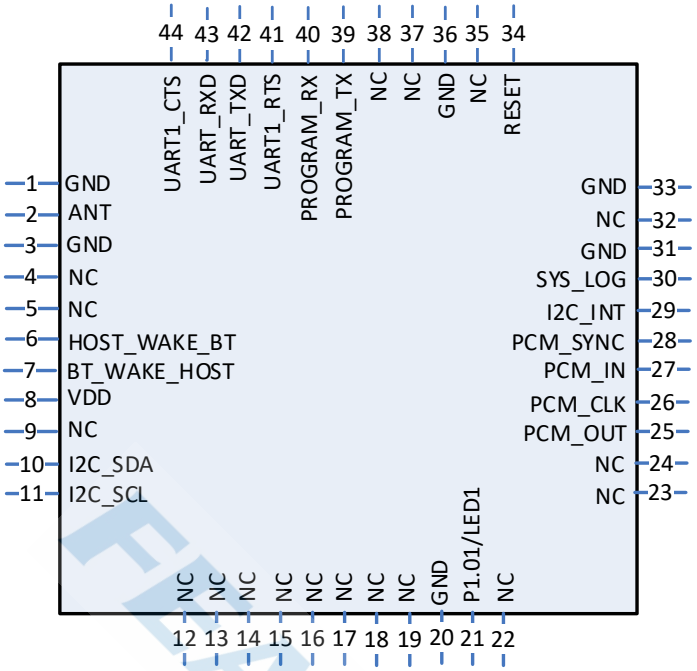


Figure 3-1-2: FSC-BT2002RV PIN Diagram (Top View)

3.2 Module Package Type

LGA package, as shown in the figure below.

Figure 3-2-1: FSC-BT2002RV Package Module Appearance

3.3 PIN Definition Descriptions

Table 3-2-1： Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	ANT	RF	Bluetooth transmit/receive (Optional)	
3	GND	Vss	Power Ground	
4	NC		Floating (Don't connected to ground)	
5	NC		Floating (Don't connected to ground)	
6	HOST_WAKE_BT	I/O	Programmable I/O	
7	BT_WAKE_HOST	I/O	Programmable I/O	
8	VDD	VDD	3.0V~3.6V	
9	NC		Floating (Don't connected to ground)	
10	I2C_SDA	I/O	I2C_SDA Alternative function: Programmable I/O	
11	I2C_SCL	I/O	I2C_SCL Alternative function: Programmable I/O	
12	NC		Floating (Don't connected to ground)	
13	NC		Floating (Don't connected to ground)	
14	NC		Floating (Don't connected to ground)	
15	NC		Floating (Don't connected to ground)	
16	NC		Floating (Don't connected to ground)	
17	NC		Floating (Don't connected to ground)	
18	NC		Floating (Don't connected to ground)	
19	NC		Floating (Don't connected to ground)	
20	GND	Vss	Power Ground	
21	P1.01/LED1	I/O	LED1 Alternative function: Programmable I/O	
22	NC		Floating (Don't connected to ground)	
23	NC		Floating (Don't connected to ground)	
24	NC		Floating (Don't connected to ground)	
25	PCM_OUT	I/O	Alternative function: I2S_DOUT/PCM_OUT Programmable I/O	
26	PCM_CLK	I/O	Alternative function: I2S_BLCK/PCM_CLK Programmable I/O	
27	PCM_IN	I/O	Alternative function:I2S_DIN/ PCM_IN Programmable I/O	
28	PCM_SYNC	I/O	Alternative function: I2S_LRCK/PCM_SYNC Programmable I/O	
29	I2C_INT	I/O	I2C_INT Alternative function: Programmable I/O	
30	SYS_LOG	I/O	SYS_LOG	

			Alternative function: Programmable I/O
31	GND	Vss	Power Ground
32	NC		Floating (Don't connected to ground)
33	GND	Vss	Power Ground
34	RESET	I	RESET System rest input with pull high, low active with at least 8ms low to trigger system rest
35	NC		Floating (Don't connected to ground)
36	GND	Vss	Power Ground
37	NC		Floating (Don't connected to ground)
38	NC		Floating (Don't connected to ground)
39	PROGRAM_TX	I/O	Program_IO2(Program_TX): Download program port
40	PROGAM_RX	I/O	Program_IO1(Program_RX): Download program port
41	UART_RTS	I/O	UART_RTS Alternative function 1: Programmable I/O
42	UART_TXD	O	UART_TXD Alternative function 1: Programmable I/O
43	UART_RXD	I	UART_RXD Alternative function 1: Programmable I/O
44	UART_CTS	I/O	UART_CTS Alternative function 1: Programmable I/O

Notice: PWR=Power Input(3.0V~3.6V); $VDD_{I/O}$=Bi-directional(3.0V~3.6V); I=Input; O=Output; RF=RF Pin; GND=Ground; F=Floating (Not Connected)

4 ELECTRICAL CHARACTERISTICS

4.1 DC Characteristic

Table 4-1-1： Power Supply Characteristics

Parameter	Min	Type	Max	Unit
Operating Temperature	-40	25	85	℃
VDD_3V3	3.0	3.3	3.6	V
$VDD_{I/O}$	3.0	3.3	3.6	V

5 PHYSICAL INTERFACE

5.1 UART Interface Characteristics

The FSC-BT2002RV UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. It supports H4 HCI interface.

The default baud rate is 115.2K baud. In order to support high and low speed baud rates, FSC-BT2002RV provides multiple UART clocks.

Table 4-1：Possible UART Settings

Parameter	Possible Values
Baud rate	Maximum – 4M bps Standard 115.2k bps Minimum – 1.2K bps
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5.1.1 UART Interface Timing

The interface includes four signals, TXD/RXD/CTS/RTS. Flow control between the host and the device is byte-wise by hardware. When the HCI_CTS signal is set high, the device stops transmitting on the interface.
If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

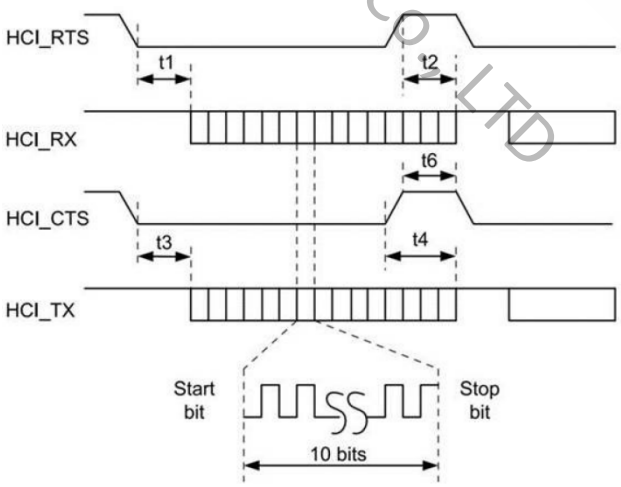


Figure 5-1-1-1: UART Timing Diagram

Table 5-2-1-1： UART Timing Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	Baud rate		115.2		3000	Kbps
	Baud rate accuracy per	Receive/Transmit	-3		3	%
T3	CTS low to TX_DATA on		0	2		ns
T4	CTS high to TX_DATA off	Hardware flow			1	byte
T6	CTS High Pulse Width		1			bit
T1	RTS low to RX DATA on		0	2		ns
T2	RST high to RX_DATA off				1	HCI packet*

Note: HCI packet means HCI command (256 bytes), HCI event (256 bytes), ACL (1024 bytes), SCO (256 bytes).

5.2 PCM Interface Characteristics

The RTL8761 supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit/16-bit linear PCM formats
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

5.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data.
FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (see Figure 5-2-1).
FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (see Figure 5-2-2).

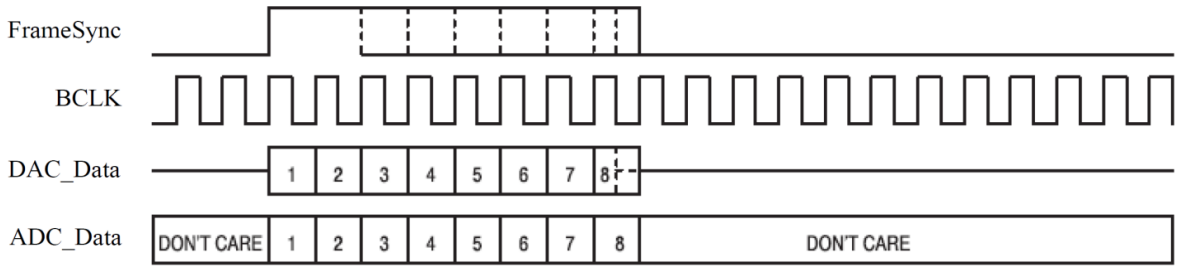


Figure 5-2-1-1: Long FrameSync

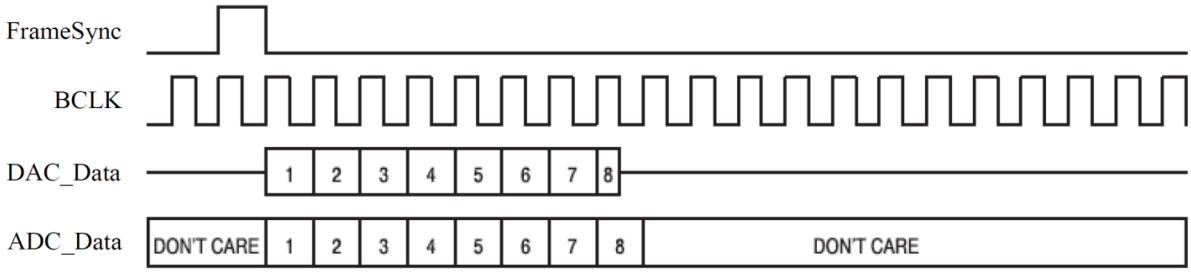


Figure 5-2-1-2: Short FrameSync

5.3 Power off by 3.3V supply power sequence

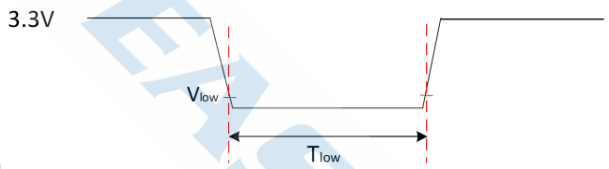


Figure 5-3-1: Power Off by RESET Sequence

Table 5-5-1: Power Off by 3.3V supply power Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{low}	Supply power keep low duration	8	100	-	ms
V_{low}	Low power threshold	-	-	0.4	V

FSC-BT2002RV can be powered off by cutting off the 3.3V power supply. The keeping low duration must be more than T_{low} and the voltage must be less than V_{low}.

6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30℃/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice (注意) :

The Feasycom's module must be used with a Step-Stencil. It is suggested to use a stencil thickness of approximately 0.16-0.2mm, which can be modified according to the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to facilitate easy manufacturing, including reflow soldering onto a PCB. However, it is the customer's responsibility to select the suitable solder paste and ensure that the oven temperatures during reflow meet the requirements specified by the solder paste manufacturer. Feasycom surface mount modules comply with the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

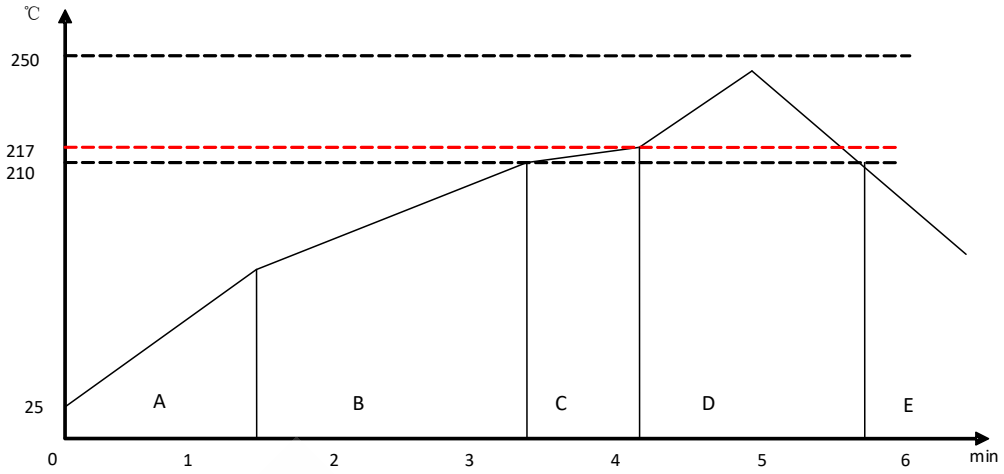


Figure 7-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 12mm(W) x 12mm(L) x 1.8mm(H) Tolerance: ±0.2mm (without shielding cover)

  12mm(W) x 12mm(L) x 2.4mm(H) Tolerance: ±0.2mm (with shielding cover)
- Module size: 12mm x 12mm Tolerance: ±0.2mm
- Pad size: 0.8mm x 0.6mm Tolerance: ±0.1mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm

(分板后边角残留板边误差：≤0.5mm) (Residual plate edge error: ≤0.5mm)

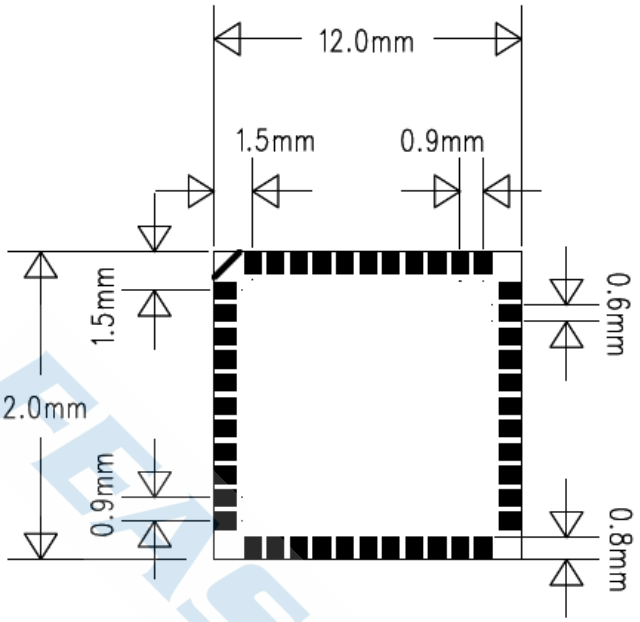


Figure 8-1-1：FSC-BT2002RV footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT2002RV is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

9.2 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

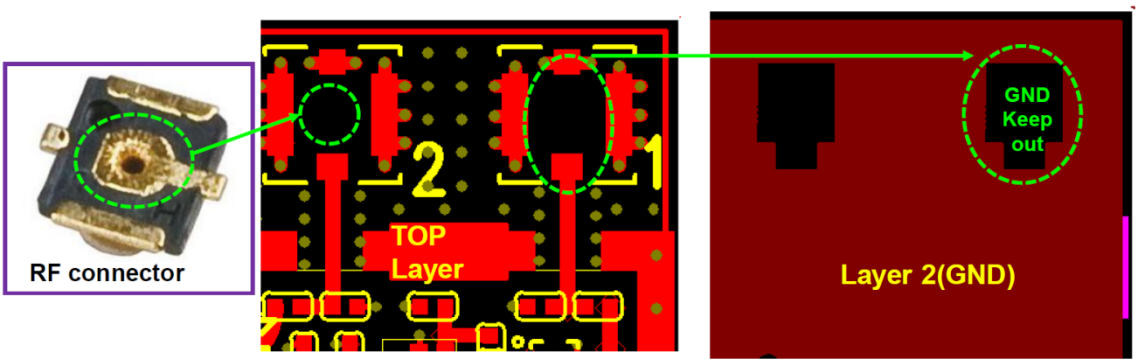


Figure 9-2-1: RF Circuit- RF pads

9.3 Recommendable antenna & IPEX by Feasycom

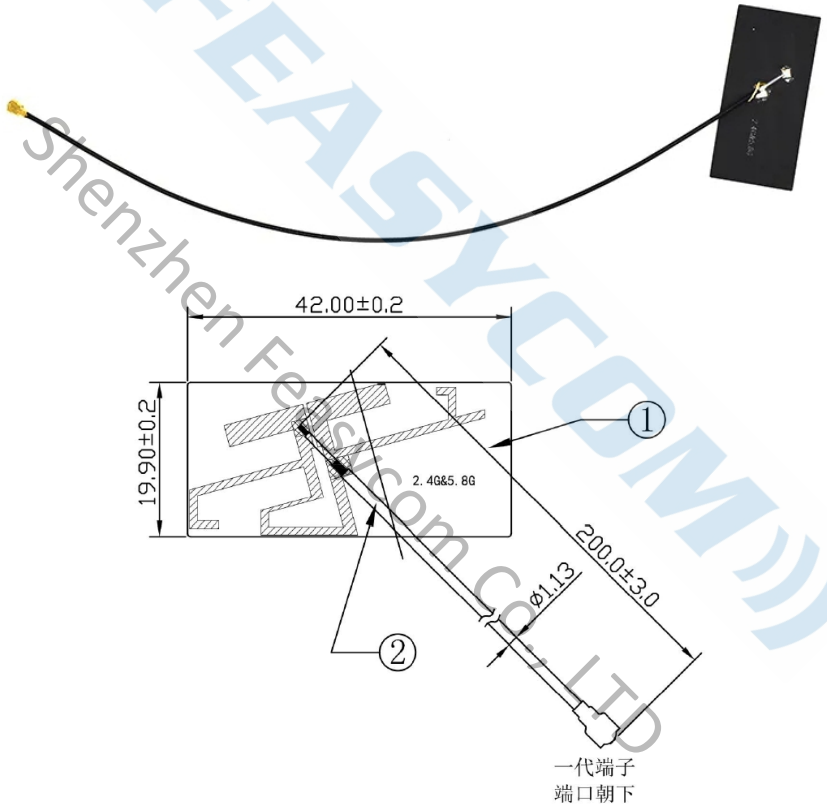
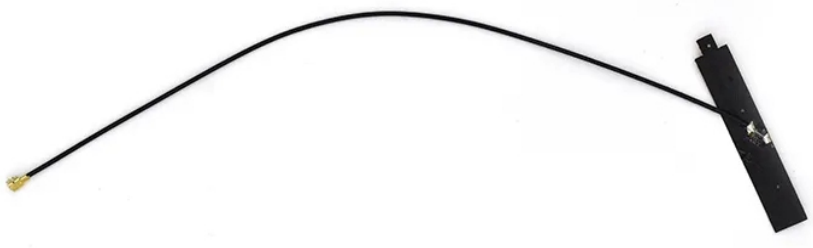


Figure 9-3-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface



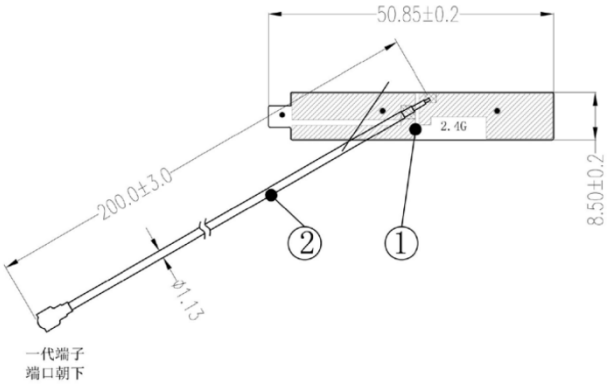
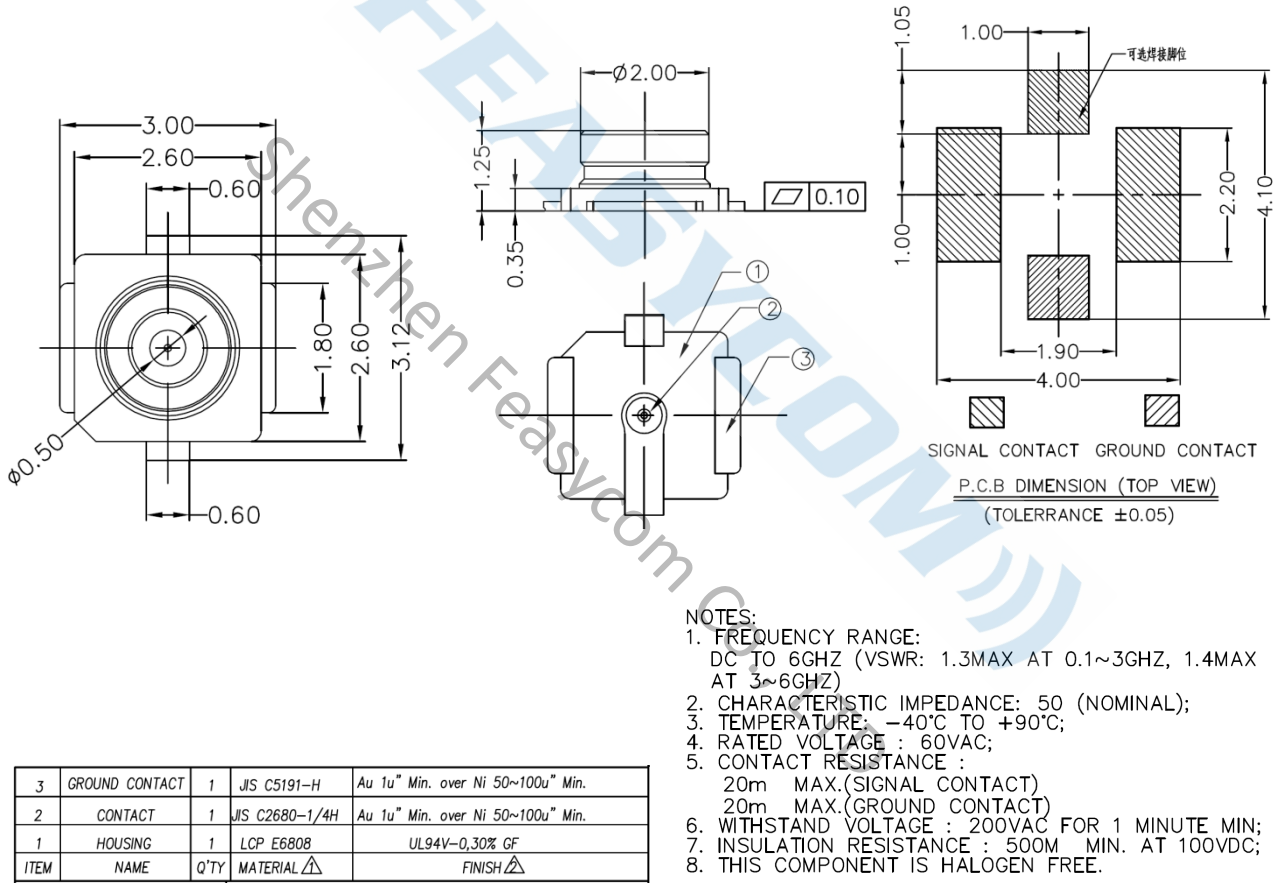


Figure 9-3-2: 2.4GHz antenna with IPEX first generation interface



ITEM	NAME	Q'TY	MATERIAL ⚠1	FINISH ⚠2
3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40℃ TO +90℃;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 9-3-3: IPEX first generation interface

9.4 Soldering Recommendations

FSC-BT2002RV is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum

profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.5 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

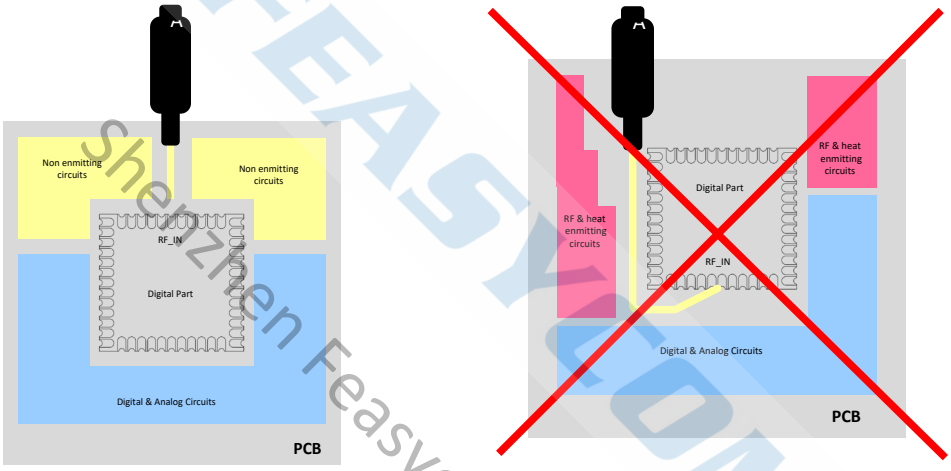


Figure 9-5-1: Placement the Module on a System Board

9.5.1 Antenna Connection and Grounding Plane Design

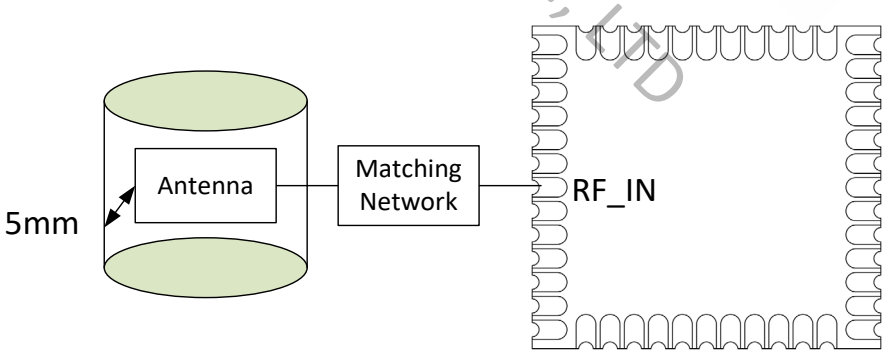


Figure 9-6-1-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

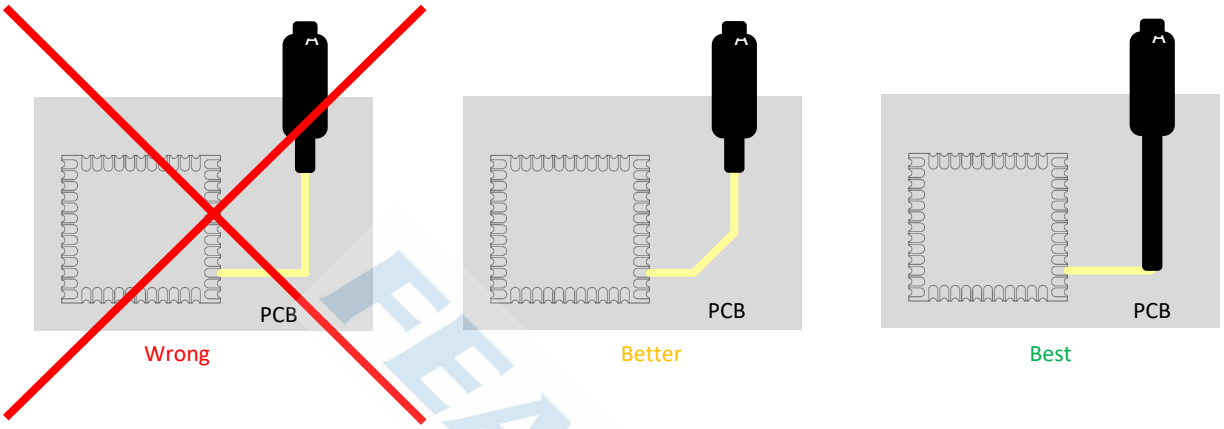


Figure 9-6-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.6 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

9.7 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 20mil

9.8 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BT2002RV Module Ground Pads

Decoupling Capacitors close to FSC-BT2002RV Module Power and Ground Pads

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 180mm* 8mm

Figure 10-1-1: Tray vacuum

10.2 Packing box (Optional)

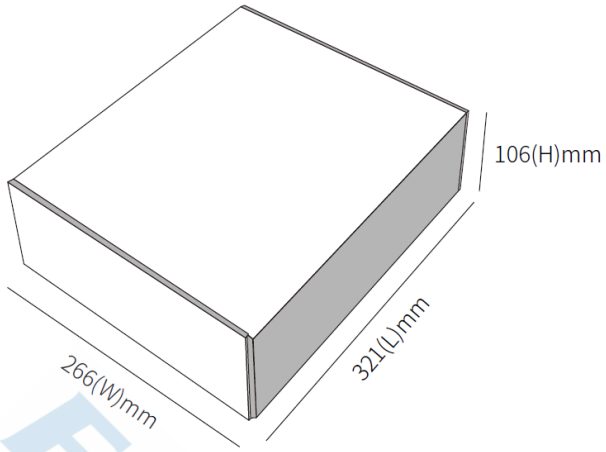


Figure 10-2-1: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

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