FSC-BT2044GI

DATASHEET V1.0

Revision History

Version	Data	Notes	Author
V1.0	2026-01-6	Initial Version	Xianjian Mo

Contact Us

Shenzhen Feasycom Co.,Ltd
Email: sales@feasycom.com
Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District,Shenzhen,518100,China.
Tel: 86-755-27924639

1 INTRODUCTION

Overview

FSC-BT2044GI supporting Bluetooth low energy (BLE)5.1 and SIG Mesh.

By default, FSC-BT2044GI module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT2044GI provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- **Low power comparator**
  - Radio receive current: 3.8 mA@3.3 V
  - Radio transmit current: 4.2 mA @0 dBm/3.3 V
  - Sleep mode (48 KB RAM retention): 1.4 μA@3 V
  - PD mode: 130 nA
- **RF Specification**
  - RX sensitivity: -95 dBm @BLE 1 Mbps
  - RX sensitivity: -92 dBm @BLE 2 Mbps
  - Power of programmable transmitter: up to +8 dBm
  - Single end antenna
- **Clock**
  - HSE: 32 MHz high speed external crystal
  - LSE: 32.768 KHz low speed external crystal
  - HSI: high speed internal RC 64 MHz

Application

- Bluetooth KEY
- OBU
- Bluetooth voice remote controller
- Smart home
- data transmission module

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth V5.1
	Frequency Band	2402MHz ~ 2480MHz
	Interface	UART/I²S/I²C
	Transmit Power	+8 dBm (Max.)
	Receiver	-95dBm (Min.) @BLE 1Mbps
Size		12mm(W) x 17mm(L) x 1.8mm(H) Tolerance: ±0.2mm (without shielding cover) 12mm(W) × 17 mm(L) × 2.2mm(H) Tolerance: ±0.2mm (with shielding cover)
Operating temperature		-40°C ~ +85°C
Storage temperature		-40°C ~ +85°C
Supply Voltage		1.8V~3.6V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V Charge device model: Pass ±500 V

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

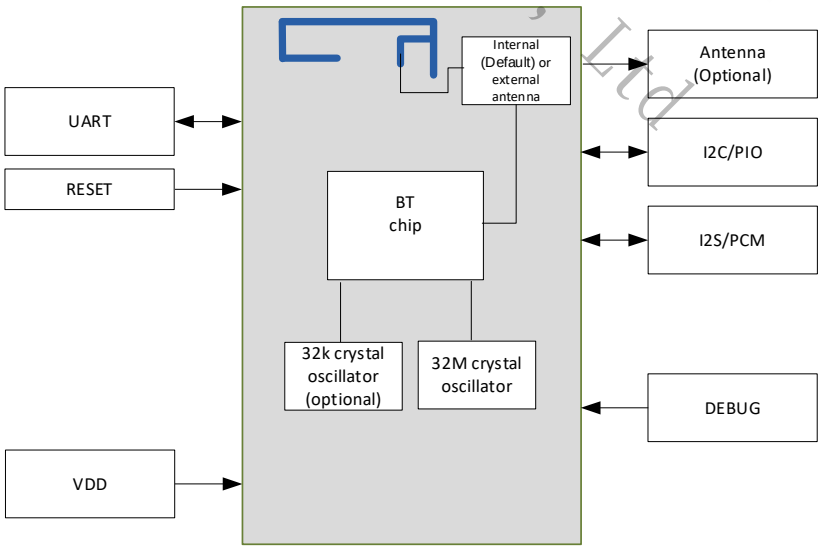

Figure 3-1-1: FSC-BT2044GI Block Diagram

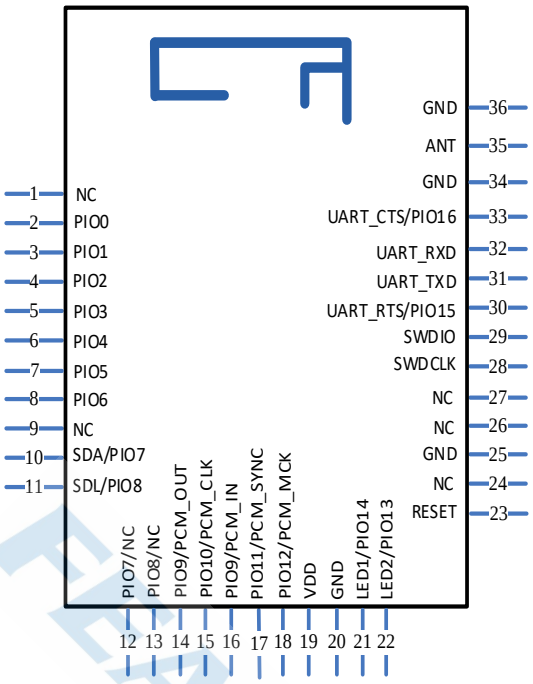

Figure 3-1-2: FSC-BT2044GI PIN Diagram (Top View)

3.2 Module Package Type

LCC package, as shown in the figure below.

Figure 3-2-1: FSC-BT2044GI Package Module Appearance

3.3 PIN Definition Descriptions

Table 3-3-1： Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	NC			
2	PIO0	I/O	Programmable I/O	
3	PIO1	I/O	Programmable I/O	
4	PIO2	I/O	Programmable I/O	
5	PIO3	I/O	Programmable I/O	
6	PIO4	I/O	Programmable I/O	
7	PIO5	I/O	Programmable I/O	
8	PIO6	I/O	Programmable I/O	
9	NC			
10	SDA/PIO7	I/O	I2C_SDA Alternative function: Programmable I/O When pin 11 is used, or an internal 32K crystal is used, this pin can only be NC	
11	SDL/PIO8	I/O	I2C_SCL Alternative function: Programmable I/O When pin 12 is used, or an internal 32K crystal is used, this pin can only be NC	
12	PIO7/NC	I/O	Programmable I/O When pin 10 is used, or an internal 32K crystal is used, this pin can only be NC	
13	PIO8/NC	I/O	Programmable I/O When pin 11 is used, or an internal 32K crystal is used, this pin can only be NC	
14	PIO9/PCM_OUT	I/O	Programmable I/O Alternative function: PCM_OUT	
15	PIO10/PCM_CLK	I/O	Programmable I/O Alternative function: PCM_CLK	
16	PIO9/PCM_IN	I/O	Programmable I/O Alternative function: PCM_IN	
17	PIO11/PCM_SYNC	I/O	Programmable I/O Alternative function: PCM_SYNC	
18	PIO12/PCM_MCK	I/O	Programmable I/O Alternative function: PCM_MCK	
19	VDD	VDD	3V3	
20	GND	VSS	Power Ground	
21	LED1/PIO14	I/O	LED1 Alternative function: Programmable I/O	
22	LED2/PIO13	I/O	LED2 Alternative function: Programmable I/O	
23	RESET	I	RESET	

24	NC		
25	GND	VSS	Power Ground
26	NC		
27	NC		
28	SWDCLK	I	DEBUG: SWDCLK Alternative function 1: Programmable I/O
29	SWDIO	I/O	DEBUG: SWDIO Alternative function 1: Programmable I/O
30	PIO15/UART_RTS	I/O	UART_RTS Alternative function 1: Programmable I/O
31	UART_TXD	O	UART_TXD Alternative function 1: Programmable I/O
32	UART_RXD	I	UART_RXD Alternative function 1: Programmable I/O
33	PIO16/UART_CTS	I/O	UART_CTS Alternative function 1: Programmable I/O
34	GND	VSS	Power Ground
35	ANT	RF	Bluetooth transmit/receive(Optional).
36	GND	VSS	Power Ground

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT2044GI UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. Supports H4 HCI interface.

Or raw UART to application. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, FSC-BT2044GI provides multiple UART clocks.

Table 4-1： Possible UART Settings

Parameter	Possible Values
Baud rate	Maximum 1M bps Standard 115200bps Minimum 1200 bps
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5 ELECTRICAL CHARACTERISTICS

5.1 DC Characteristic

Table 5-1： DC Characteristics

Parameter	Min	Type	Max	Unit
Operating Temperature	-40	25	85	℃
VDD	1.8	3.3	3.6	V
$VDD_{I/O}$	1.8	3.3	3.6	V

6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60% RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

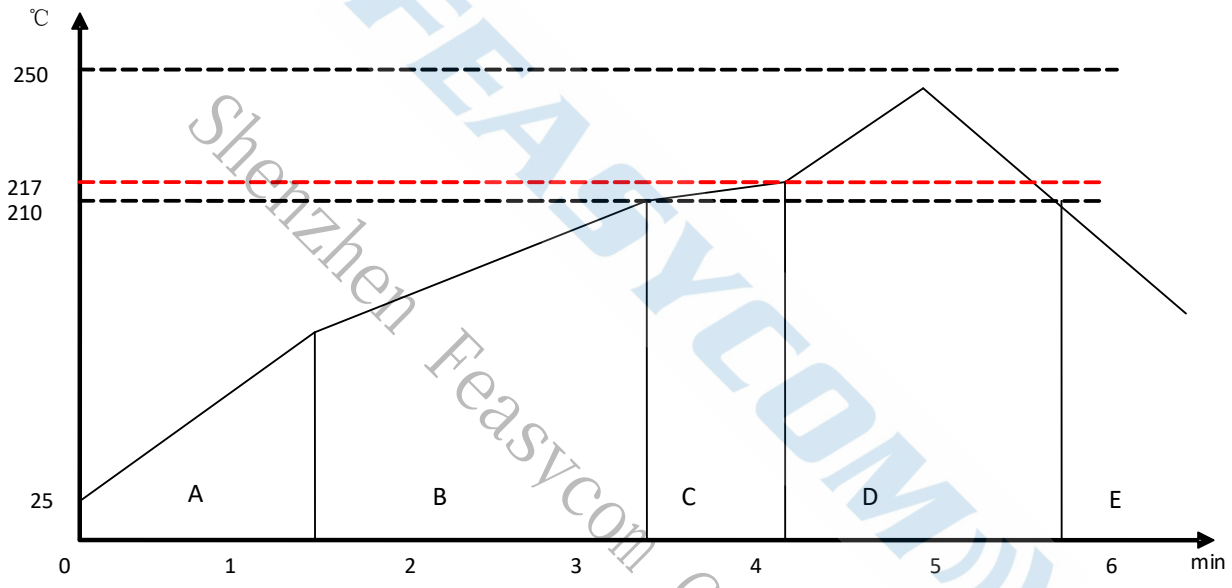

Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90

second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 12mm(W) x 17mm(L) x 1.8mm(H) Tolerance: ±0.2mm (without shielding cover)
  12mm(W) × 17 mm(L) × 2.2mm(H) Tolerance: ±0.2mm (with shielding cover)
- Module size: 12mm X 17mm Tolerance: ±0.2mm
- Pad size: 1.7mmX0.5mm Tolerance: ±0.2mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

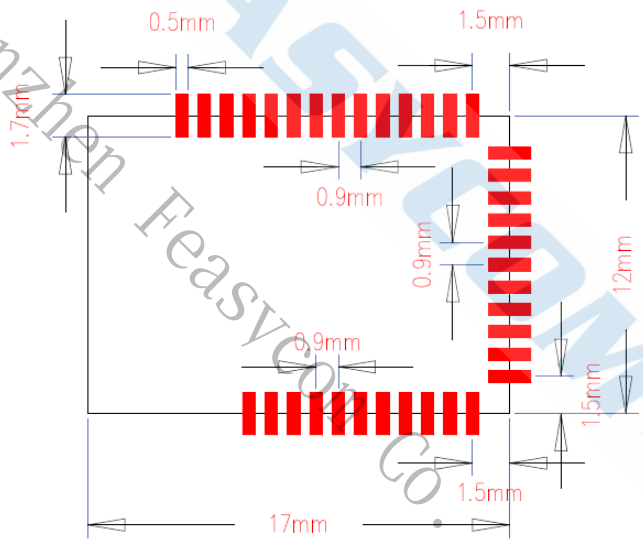

Figure 8-1： FSC-BT2044GI footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT2044GI is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

9.2 Layout Recommendations for Product Design Structure

The onboard antenna of this module is a specially designed antenna. Its optimal performance characteristics are highly dependent on the actual product's structure, materials, module placement, the shape of the baseboard, and even the thickness and dimensions of the baseboard. Therefore, the customer's baseboard design must strictly adhere to this guide to achieve the best RF performance and complete real-world distance testing and validation.

9.2.1 Module Layout Recommendations

Recommendation 1:

Place the module in the middle of the main board **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 9-2-1:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

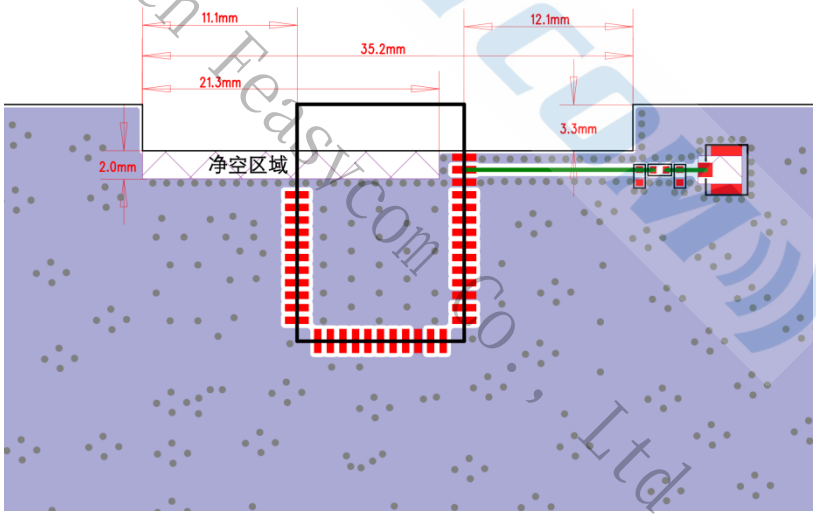

Figure 9-2-1： Module Layout - Baseboard TOP Layer

When the module is placed in the middle of the baseboard, the L2/L3/Ln...../Bottom layer layout is shown in Figure 9-2-2:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.3x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

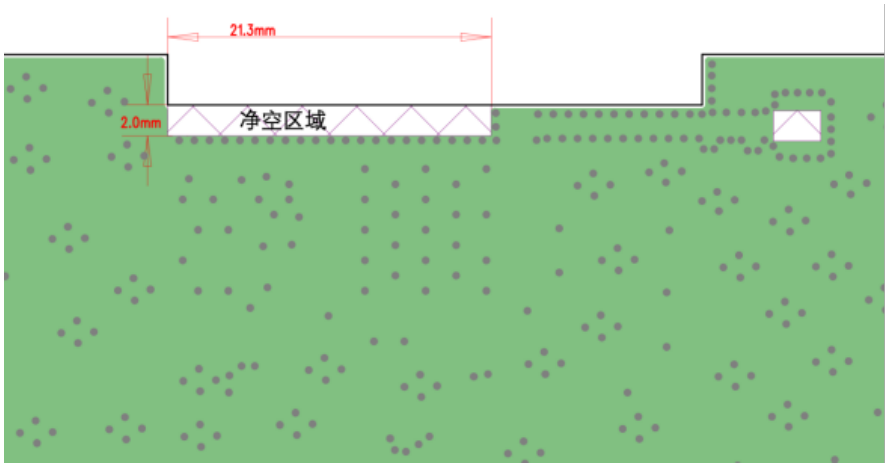

Figure 9-2-2： Module Layout - Baseboard L2/L3/BOTTOM Layers

Recommendation 2:

Similar to Recommendation 1, place the module at the edge of the baseboard **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 9-2-3:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

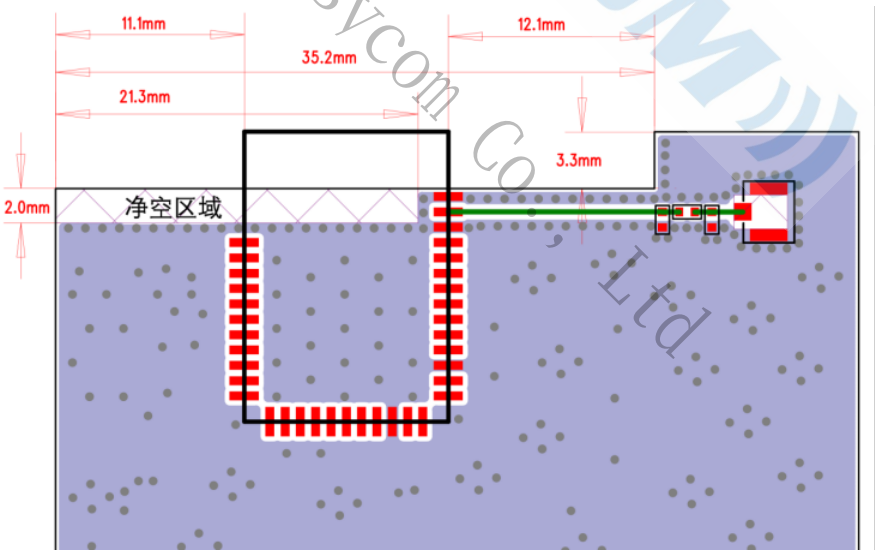

Figure 9-2-3： Module Layout - Baseboard TOP Layer

When the module is placed at the corner of the main board, the L2/L3/Ln...../Bottom layer layout is shown in Figure 9-2-4:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.23x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

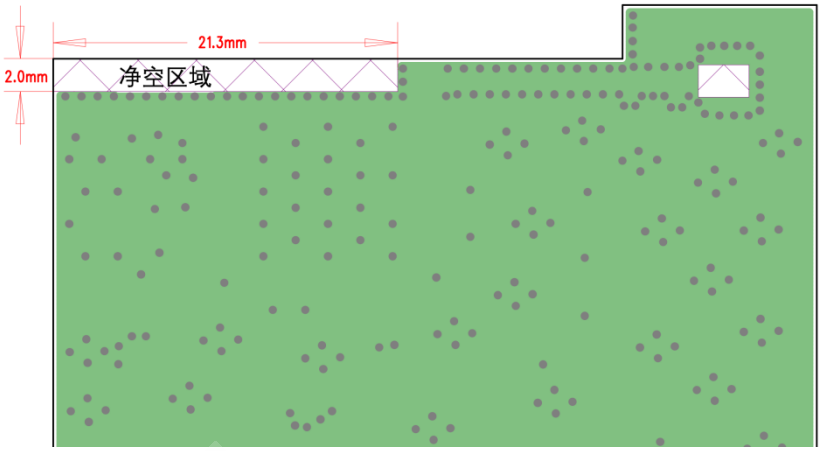

Figure 9-2-4：Module Layout - Main Board L2/L3/Ln...../BOTTOM Layers

9.2.2 Special Trace Recommendations

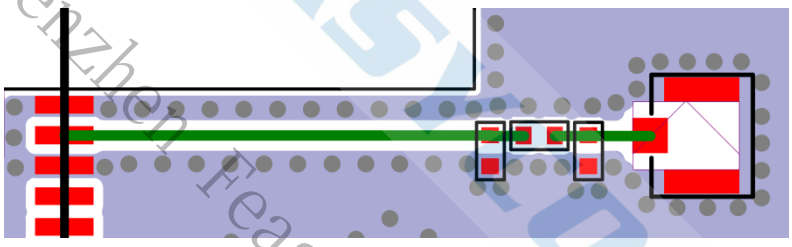

Figure 9-2-5：External Antenna Trace Schematic

The signal transmission line from the module to the antenna matching circuit should be a 50-ohm characteristic impedance microstrip line. The width of the microstrip line and the spacing from the ground copper must be determined based on the specific PCB layer stack-up. No intersecting lines are allowed between the microstrip line and the ground. All layers beneath the IPEX connector must be cleared (as shown by the purple cross-hatched area under the connector).

9.3 Layout Guidelines (External Antenna)

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antenna designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the system PCB.

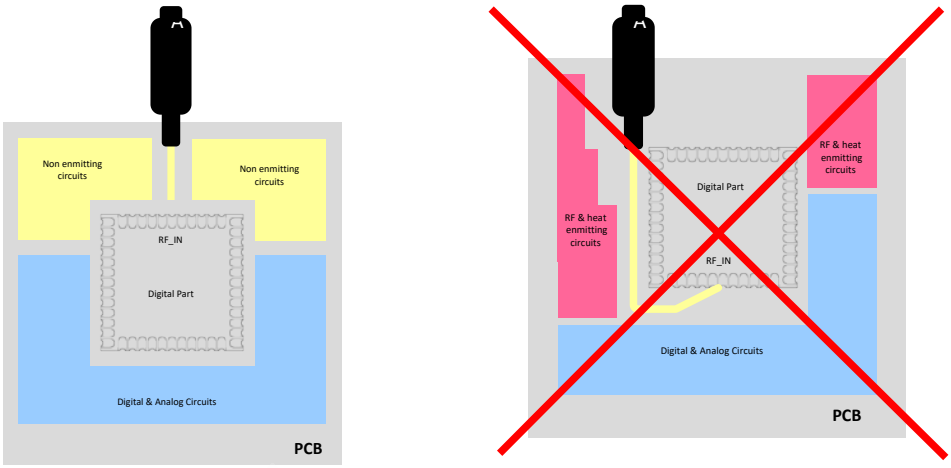

Figure 9-3-1: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

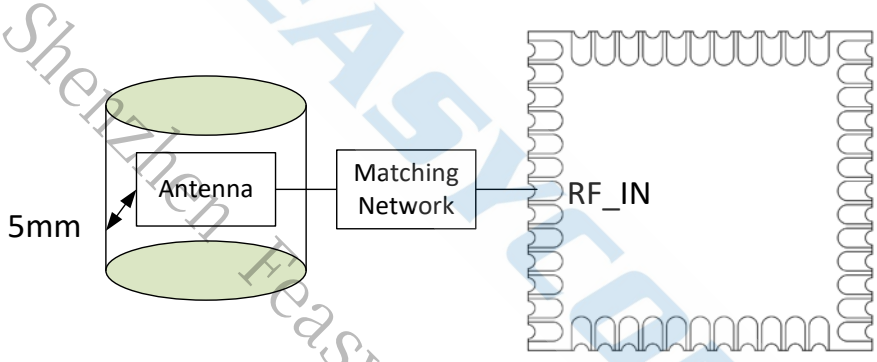

Figure 9-3-2: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should be at least as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

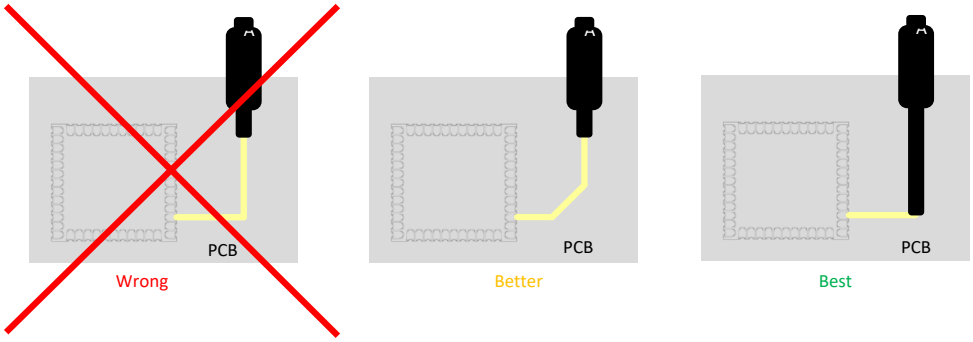

Figure 9-3-3: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 230mm * 180mm * 8mm

Figure 10-1: Tray vacuum

10.2 Packing box (Optional)

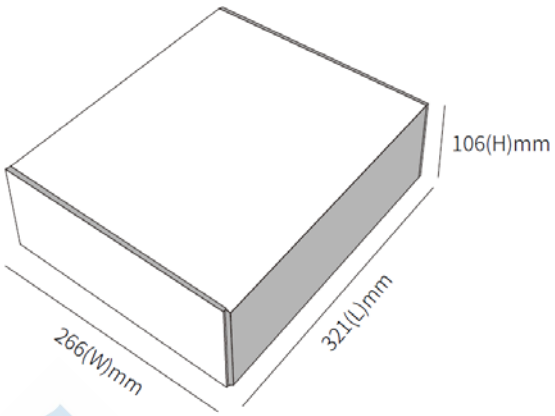

Figure 10-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

11 APPLICATION SCHEMATIC