FSC-BT2064FI

DATASHEET V1.0

Revision History

Version	Data	Notes	Author
V1.0	2025-06-26	Initial Version	Liu

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1 INTRODUCTION

Overview

FSC-BT2064FI supports Bluetooth dual-mode V5.3(BR/EDR/BLE).

By default, the FSC-BT2064FI module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over a serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT2064FI provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- **Supporting feature**:
  - Standard configurable RF transmission power -20 dBm to 2dBm
  - Low Power
  - Supports 1 Mbps/2 Mbps/3 Mbps BR/EDR
  - Supports 1 Mbps/2 Mbps LE
  - Supports long-distance transmission of LE 125Kbps/500Kbps
  - RSSI is supported
  - Dynamic TX power control
  - Bluetooth host protocol stack implemented by another MCU or host AP
- **RF Specification**:
  - RX Receiving sensitivity -88dBm (BR 1Mbps)
  - RX Receiving sensitivity -90dBm (EDR 2Mbps)
  - RX Receive sensitivity -82dBm (EDR 3Mbps)
  - RX Receive sensitivity -93dBm (LE 1Mbps)
  - RX Receiving sensitivity -90dBm (LE 2Mbps)
  - RX Receiving sensitivity -95dBm (LE LR2 1Mbps)
  - RX Receiving sensitivity -97dBm (LE LR8 1Mbps)
  - TX Transmit power -20 dBm to 2dBm

2 GENERAL SPECIFICATIONS

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth V5.3
	Frequency Band	2402MHz ~ 2480MHz
	Interface	UART/PIO/ADC/SPI
	Transmit Power	Up to 2dBm
	Receiver	-90dBm（EDR 2Mbps）
Size		12 mm × 17 mm × 2.2 mm
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Supply Voltage		3.3V~3.6V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V Charge device model: Pass ±500 V

3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and PIN Diagram

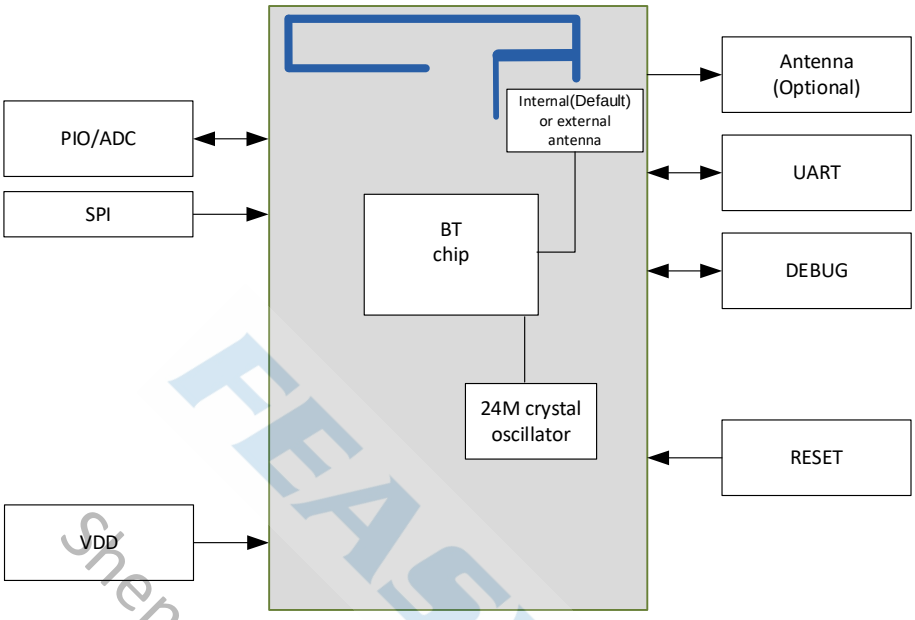


Figure 3-1-1: FSC-BT2064FI Block Diagram

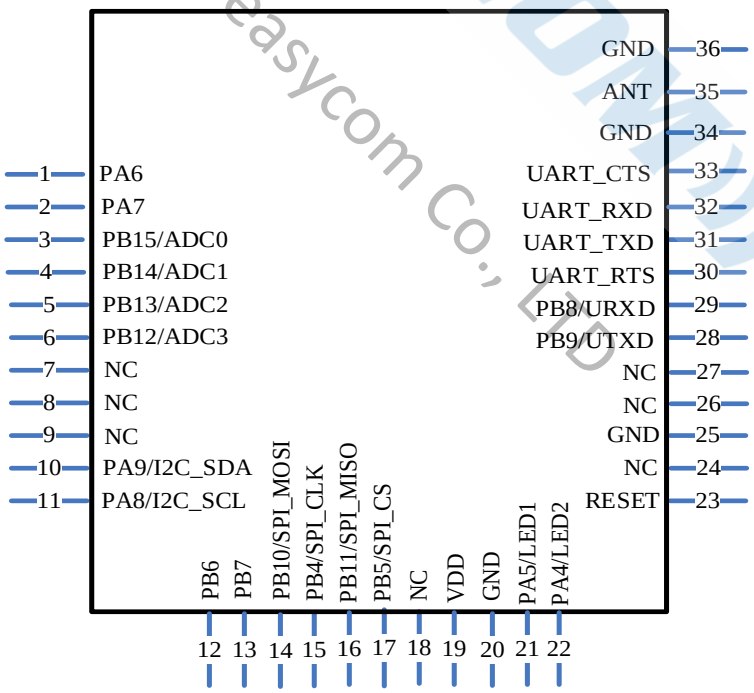


Figure 3-1-2: FSC-BT2064FI PIN Diagram (Top View)

3.2 PIN Definitions

Table 3-2：Pin definitions

Pin	Pin Name	Type	Pin Descriptions	Notes
1	PA6	I/O	Programmable input/output line	
2	PA7	I/O	Programmable input/output line	
3	PB15/ADC0	I/O	Programmable input/output line **Alternative Function 1:ADC0**	
4	PB14/ADC1	I/O	Programmable input/output line **Alternative Function 1:ADC1**	
5	PB13/ADC2	I/O	Programmable input/output line **Alternative Function 1:ADC2**	
6	PB12/ADC3	I/O	Programmable input/output line **Alternative Function 1:ADC3**	
7	NC			
8	NC			
9	NC			
10	PA9/I2C_SDA	I/O	Programmable input/output line **Alternative Function 1: I2C_SDA**	
11	PA8/I2C_SCL	I/O	Programmable input/output line **Alternative Function 1: I2C_SCL**	
12	PB6	I/O	Programmable input/output line	
13	PB7	I/O	Programmable input/output line	
14	PB10/SPI_MOSI	I/O	Programmable input/output line **Alternative Function 1: SPI_MOSI**	
15	PB4/SPI_CLK	I/O	Programmable input/output line **Alternative Function 1: SPI_CLK**	
16	PB11/SPI_MISO	I/O	Programmable input/output line **Alternative Function 1: SPI_MISO**	
17	PB5/SPI_CS	I/O	Programmable input/output line **Alternative Function 1: SPI_CS**	
18	NC			
19	VDD	VDD	Power supply voltage 3.3V~ 3.6V	
20	GND	Vss	Power Ground	
21	PA5	I/O	Programmable input/output line **Alternative Function 1: LED** **Power On: Light Slow Shinning; Connected: Steady Lighting.**	
22	PA4	I/O	Programmable input/output line **Alternative Function 1: BT Status** ***Connected: High; Not connected: low*.**	
23	RESET	I	External reset input: Active LOW. Set this pin low reset to initial state	
24	NC			

25	GND	Vss	Power Ground
26	NC		
27	NC		
28	PB9/UTXD	I/O	Firmware download TXD
29	PB8/URXD	I/O	Firmware download RXD
30	UART_RTS	I/O	UART_RTS Alternative function 1: Programmable I/O
31	UART_TXD	O	UART_TXD Alternative function 1: Programmable I/O
32	UART_RXD	I	UART_RXD Alternative function 1: Programmable I/O
33	UART_CTS	I/O	UART_CTS Alternative function 1: Programmable I/O
34	GND	Vss	Power Ground
35	ANT	RF	Bluetooth transmit/receive(Optional).
36	GND	Vss	Power Ground

4 ELECTRICAL CHARACTERISTICS

4.1 UART Interface

The FSC-BT2064FI UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. It supports H4 HCI interface.

The default baud rate is 921.6k baud. In order to support high and low speed baud rates, FSC-BT2064FI provides multiple UART clocks.

The default setting is to use H5 with a baud rate of 921600, and there is no need for flow control.

Table 4-1： Possible UART Settings

Parameter	Possible Values
Baud rate	Minimum - Standard 921600bps Maximum -
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5 MSL & ESD

Table 5-1: MSL and ESD

Parameter	Value
MSL grade	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V

6 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30℃/60% RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Note：

The Feasycom's module must be used with a Step-Stencil. It is suggested to use a stencil thickness of approximately 0.16-0.2mm, which can be modified according to the product.

Table 6-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to facilitate easy manufacturing, including reflow soldering onto a PCB. However, it is the customer's responsibility to select the suitable solder paste and ensure that the oven temperatures during reflow meet the requirements specified by the solder paste manufacturer. Feasycom surface mount modules comply with the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

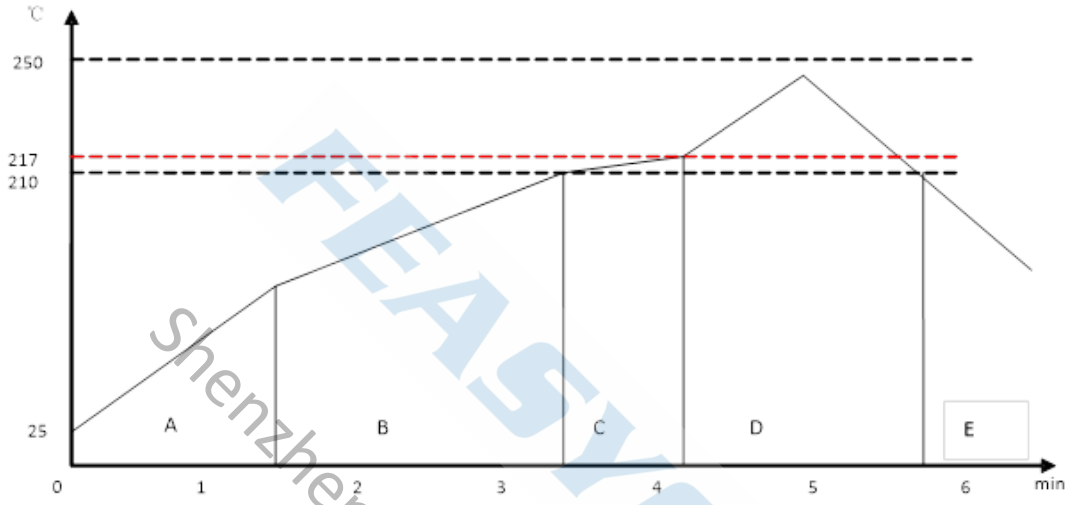


Figure6-1-1： Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate, usually **ranging from 0.5 to 2 °C/s**. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. **For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.**

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

7 MECHANICAL DETAILS

7.1 Mechanical Details

- Dimension: 12mm(W) x 17mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 12mm X 17mm Tolerance: ±0.2mm
- Pad size: 1.7mmX0.5mm Tolerance: ±0.2mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

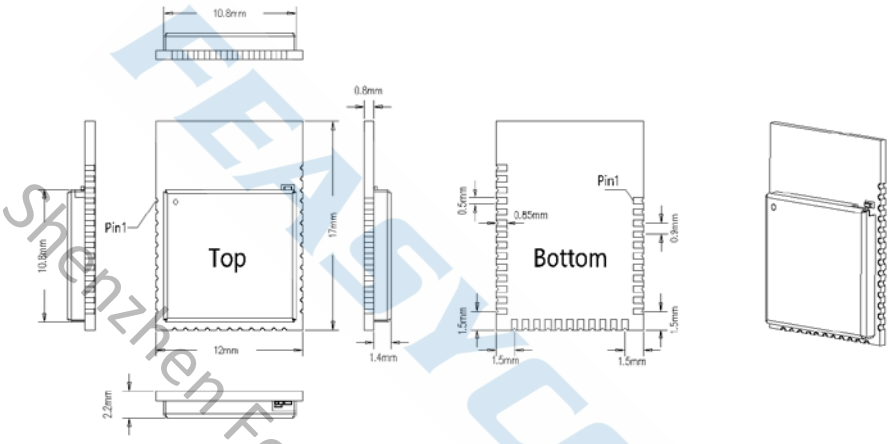


Figure 7-1-1：FSC-BT5003RV package dimensions diagram

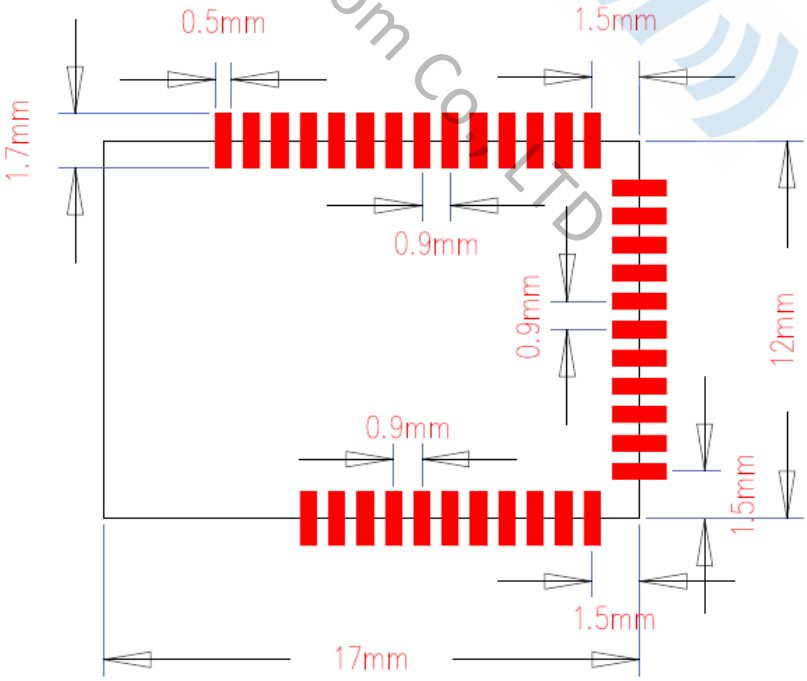


Figure 7-1-2：FSC-BT2064FI footprint Layout Guide (Top View)

8 HARDWARE INTEGRATION SUGGESTIONS

8.1 Soldering Recommendations

FSC-BT2064FI is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

8.2 Layout Recommendations for Product Design Structure

The onboard antenna of this module is a specially designed antenna. Its optimal performance characteristics are highly dependent on the actual product's structure, materials, module placement, the shape of the baseboard, and even the thickness and dimensions of the baseboard. Therefore, the customer's baseboard design must strictly adhere to this guide to achieve the best RF performance and complete real-world distance testing and validation.

8.2.1 Module Layout Recommendations

Recommendation 1: Place the module in the middle of the main board **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 8-2-1:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

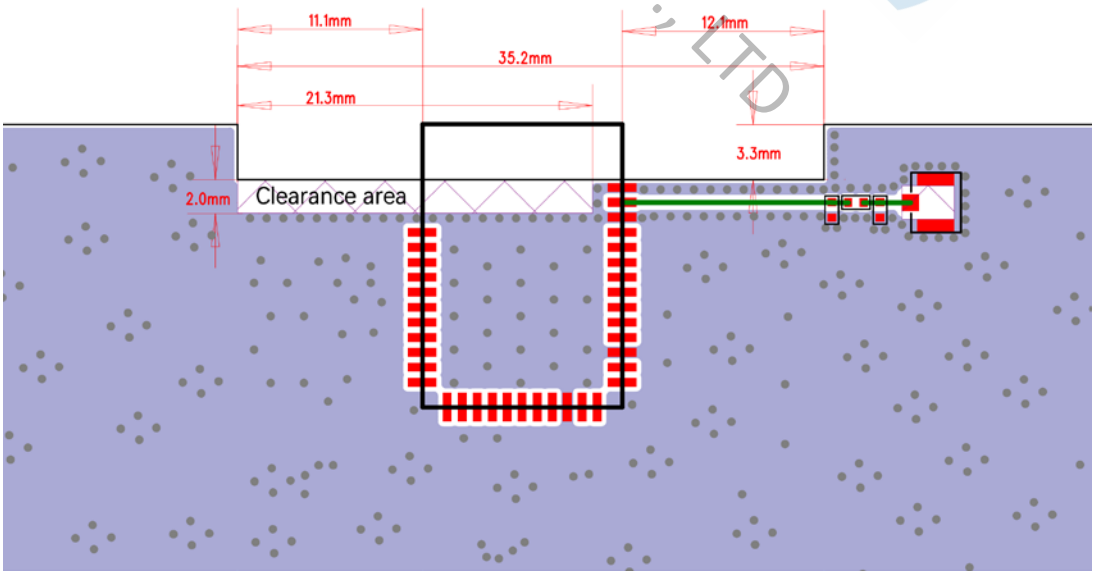


Figure 8-2-1：Module Layout - Baseboard TOP Layer

When the module is placed in the middle of the baseboard, the L2/L3/Ln...../Bottom layer layout is shown in Figure 8-2-2:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.3x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

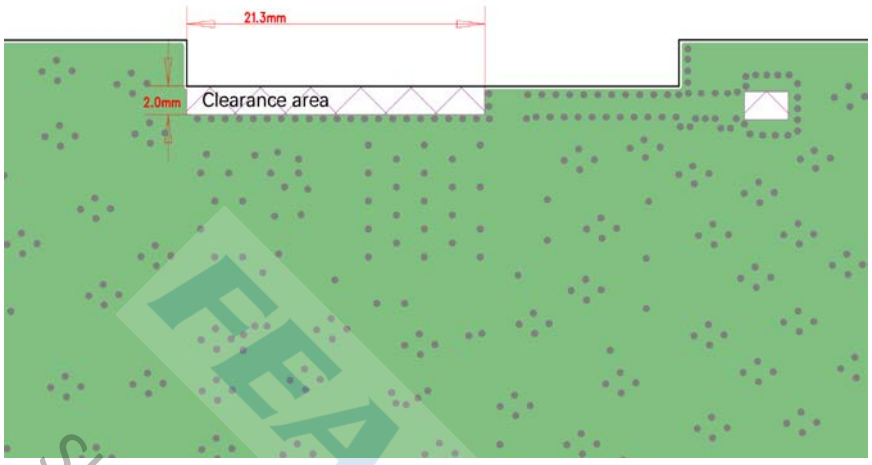


Figure 8-2-2： Module Layout - Baseboard L2/L3/BOTTOM Layers

Recommendation 2: Similar to Recommendation 1, place the module at the edge of the baseboard **(the customer's baseboard must be hollowed out)**. The TOP layer layout is shown in Figure 8-2-3:

- The upper edge of the module should align with the edge of the baseboard.
- The left edge of the module should be 11.1mm from the board edge, and the right edge of the module should be 12.1mm from the hollowed edge of the baseboard.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.
- The hollowed-out area on the baseboard should measure 35.2x3.3mm.
- The clearance area on the baseboard should measure 21.3x2.0mm.

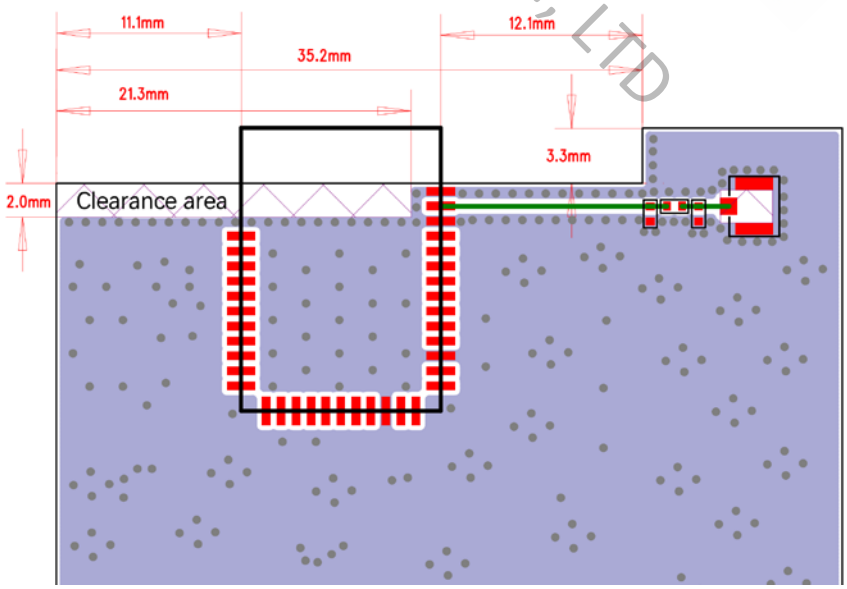


Figure 8-2-3： Module Layout - Baseboard TOP Layer

When the module is placed at the corner of the main board, the L2/L3/Ln...../Bottom layer layout is shown in Figure 8-2-4:

- The clearance area on L2/L3/Ln...../Bottom layers should measure 21.23x2.0mm.
- No copper pour or traces are allowed on any layers beneath the IPEX connector.

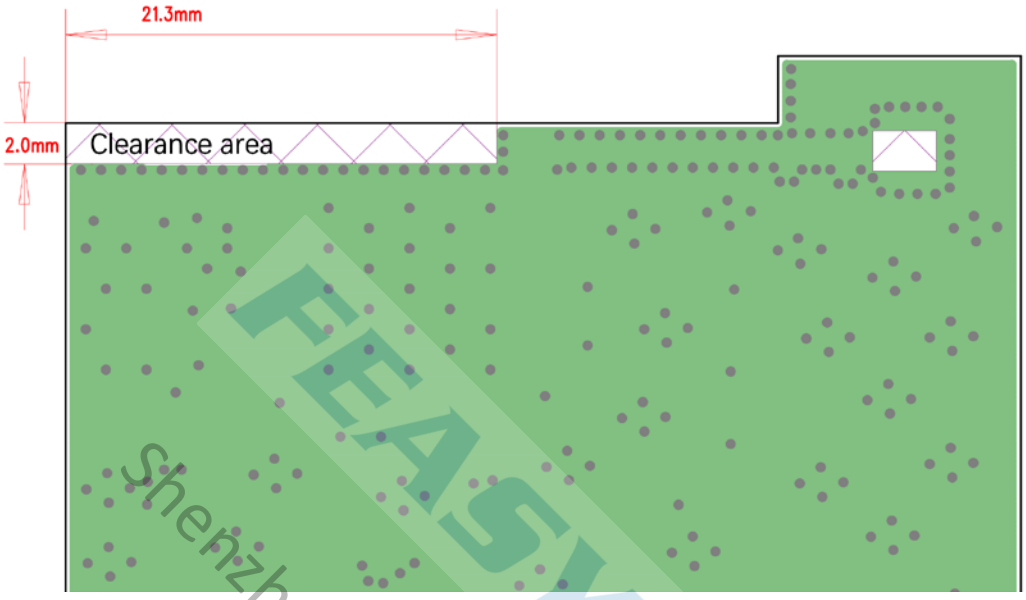


Figure 8-2-4: Module Layout - Main Board L2/L3/Ln...../BOTTOM Layers

8.2.2 Special Trace Recommendations

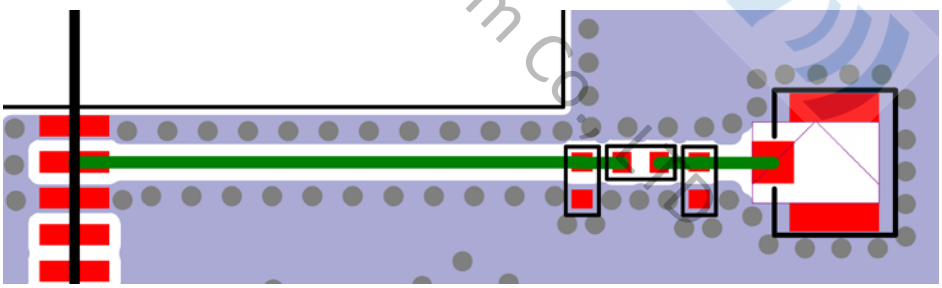


Figure 8-2-5： External Antenna Trace Schematic

The signal transmission line from the module to the antenna matching circuit should be a 50-ohm characteristic impedance microstrip line. The width of the microstrip line and the spacing from the ground copper must be determined based on the specific PCB layer stack-up. No intersecting lines are allowed between the microstrip line and the ground. All layers beneath the IPEX connector must be cleared (as shown by the purple cross-hatched area under the connector).

8.3 Layout Guidelines (External Antenna)

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antenna designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the system PCB.

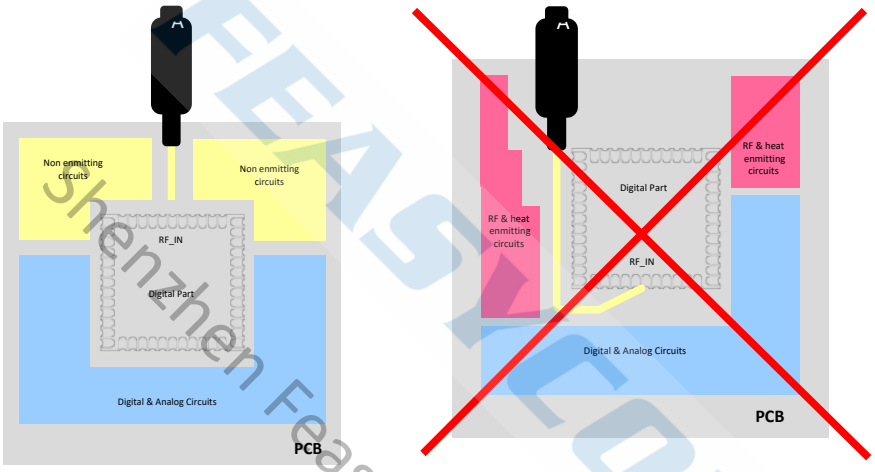


Figure 8-3-1: Placement the Module on a System Board

8.3.1 Antenna Connection and Grounding Plane Design

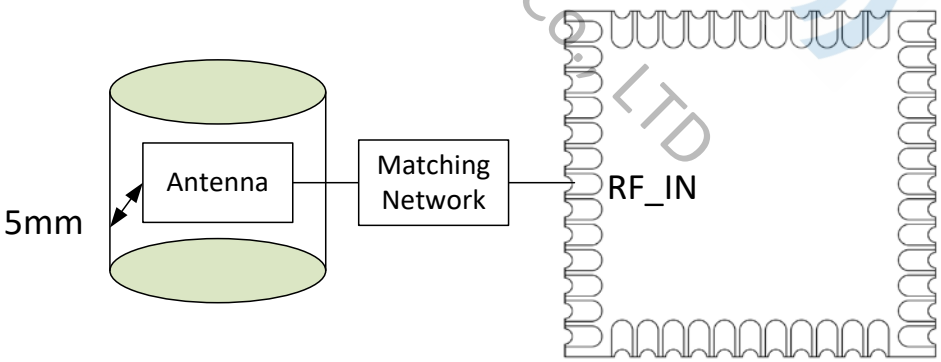


Figure 8-3-1-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should be at least as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

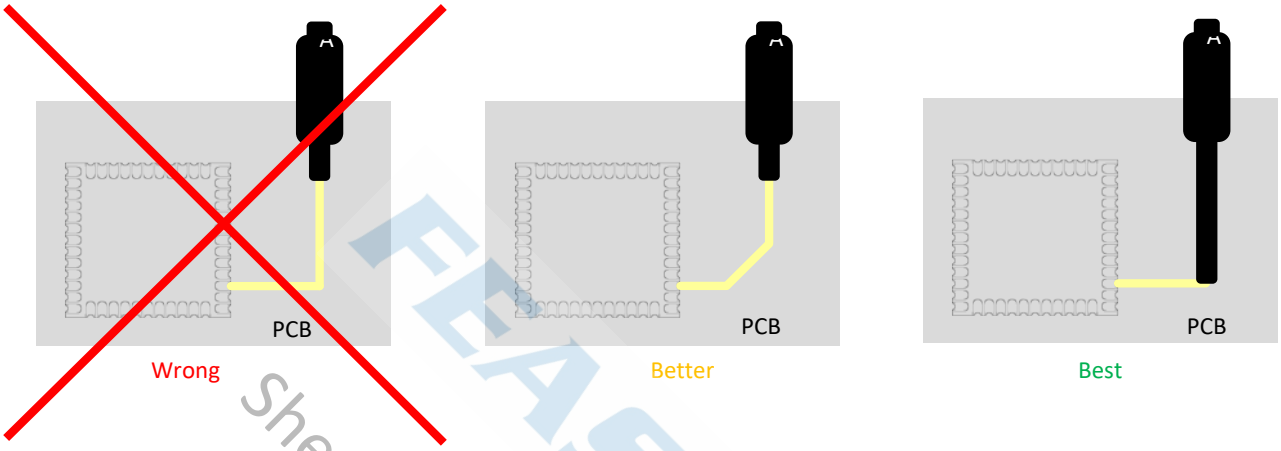


Figure 8-3-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9 PRODUCT PACKAGING INFORMATION

9.1 Default Packing

Figure 9-1-1: Tray vacuum

9.2 Packing box (Optional)

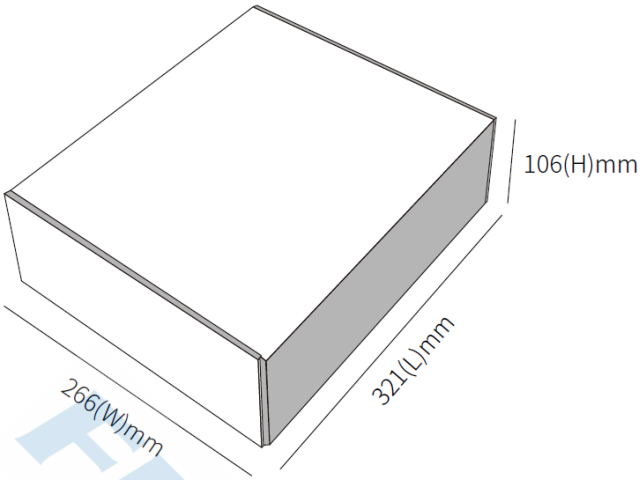


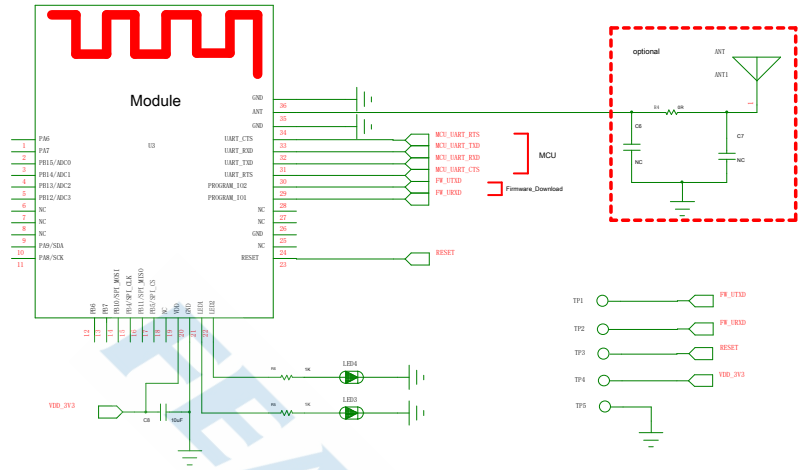
Figure 9-2-1: Packing box (Optional)

** If any packaging other than the package mentioned above is required, please confirm the packaging size again..*

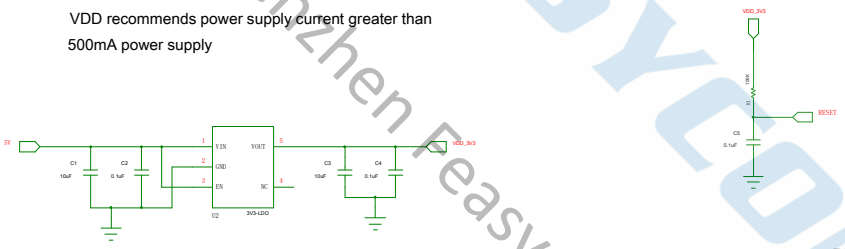
** Packing: 1000pcs per carton (Minimum packing quantity).*

** The outer packing size provided above is for reference purposes only. For the actual dimensions of the product's packaging, please refer to the packaging of the actual goods.*

10 APPLICATION SCHEMATIC



VDD recommends power supply current greater than 500mA power supply



POWER

RESET