FSC-BT825B

Bluetooth 5.3 Dual Mode Module Data Sheet

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Release Record

Version Number	Release Date	Comments
Revision 1.0	2019-08-03	First Release
Revision 1.1	2019-10-10	Add certificate picture
Revision 1.2	2020-07-20	Increase chip model
Revision 1.2.1	2021-09-23	Update package drawing
Revision 1.2.2	2022-05-09	Add FTP profile
Revision 1.2.3	2022-08-12	Change the operating temperature: 0ºC to +70 ºC
Revision 1.3	2023-08-11	Update operating temperature -20ºC to +85 ºC, Bluetooth version V5.3
Revision 1.4	2024-07-04	Update Chapter 6

1. INTRODUCTION

The FSC-BT825B is a fully integrated Bluetooth module that complies with the Bluetooth 5.3 specification dual mode protocol (BR / EDR / BLE). It supports SPP, BLE, FTP, ANCS, iBeacon configuration files. It integrates the baseband controller in a small package and supports an external antenna, so designers can have more flexibility in product shape.

FSC-BT825B can be communicated by UART port. With Feasycom's Bluetooth stack, Customers can easily transplant to their software. Please refer to Feasycom stack design guide.

1.1 Block Diagram

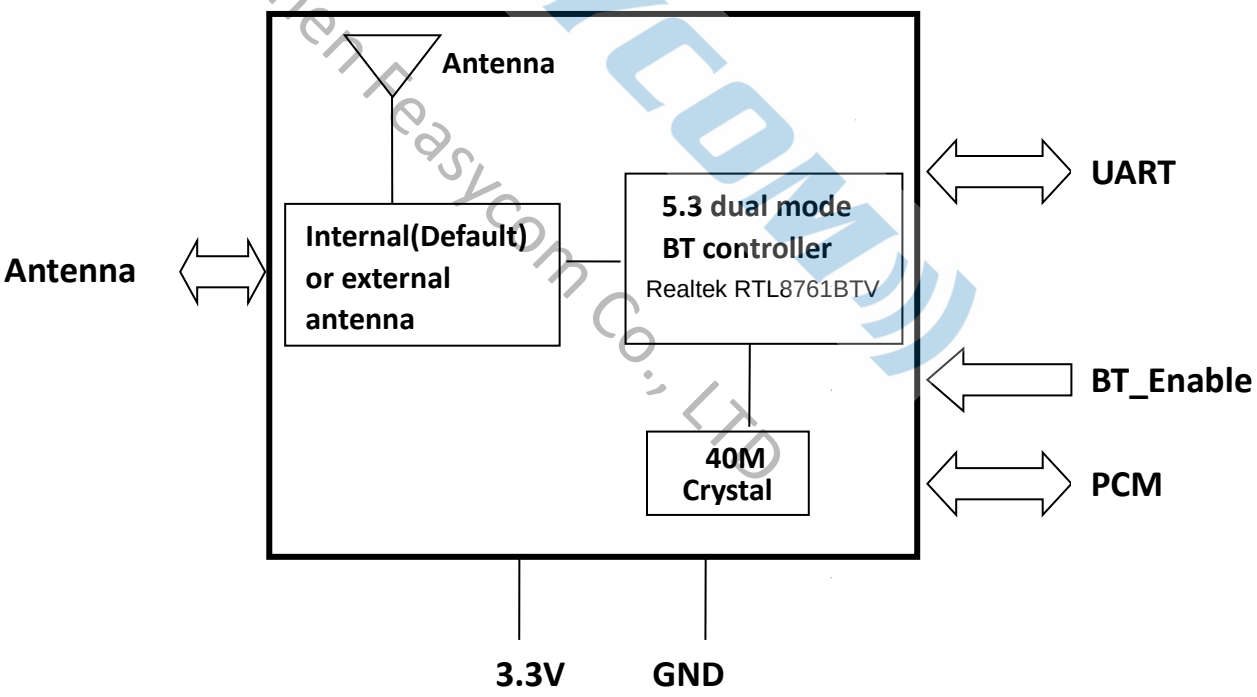

Figure 1

1.2 Feature

- Bluetooth 5.3 specification compliant
- Postage stamp sized form factor, 10.8mm x 13.5mm x 1.8mm
- Supports TX +10dBm maximum output power for Bluetooth BR/BLE
  Supports TX +7.5dBm maximum output power for Bluetooth EDR
- Receive sensitivity: -94 dBm(2Mbps EDR Minimum)
  -98 dBm(BLE Minimum)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921.6Kbps
- UART, PCM data connection interfaces.
- Bluetooth stack profiles support: SPP, HFP/HSP, A2DP, AVRCP, MAP, FTP and all BLE protocols.

1.3 Applications

- Smart Watch and Bluetooth Bracelet
- Health & Medical devices
- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset tacking

2. GENERAL SPECIFICATION

General Specification	
Chip Set	RTL8761BTV
Product ID	FSC-BT825B
Dimension	10.8mm(W) x 13.5mm(L) x 1.8mm(H)
Bluetooth Specification	Bluetooth V5.3 (Dual Mode)
Power Supply	3~3.6 Volt DC
Output Power	+4.5 dBm (default for all data rate) +10 dBm (BR/BLE)(Max.) +7.5 dBm (EDR)(Max.)
Sensitivity	-94 dBm(2Mbps EDR)(Min.) -98 dBm(BLE)(Min.)
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	GFSK, π/4-DQPSK, 8-DPSK
Baseband Crystal OSC	40MHz
Hopping & channels	1600hops/sec, 1MHz channel space,79 Channels(BT 5.x to 2MHz channel space)
RF Input Impedance	50 ohms
Antenna	Internal (Default) External (Option)
Interface	Data: UART Audio: PCM
Profile	SPP, BLE (Standard),FTP, ANCS, HFP, A2DP, AVRCP, MAP(optional)
Temperature	-20ºC to +85 ºC
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

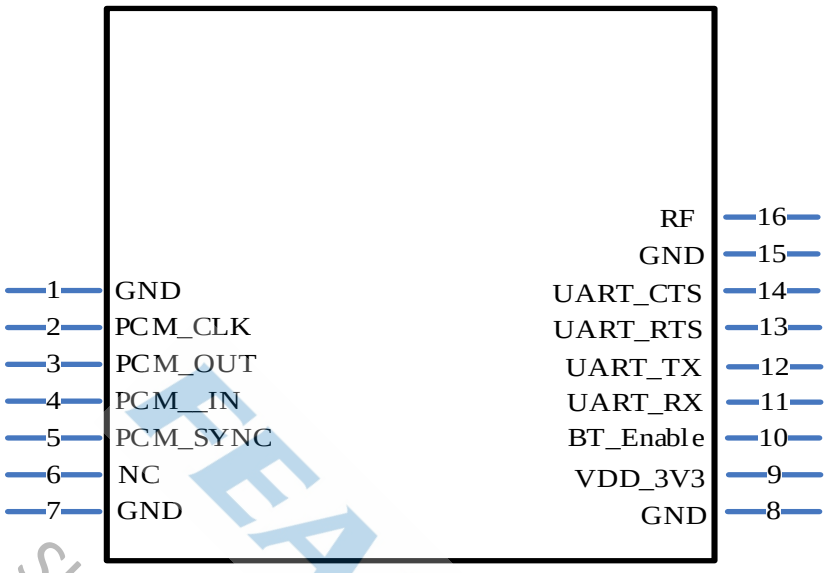

Figure 2: FSC-BT825B PIN Diagram

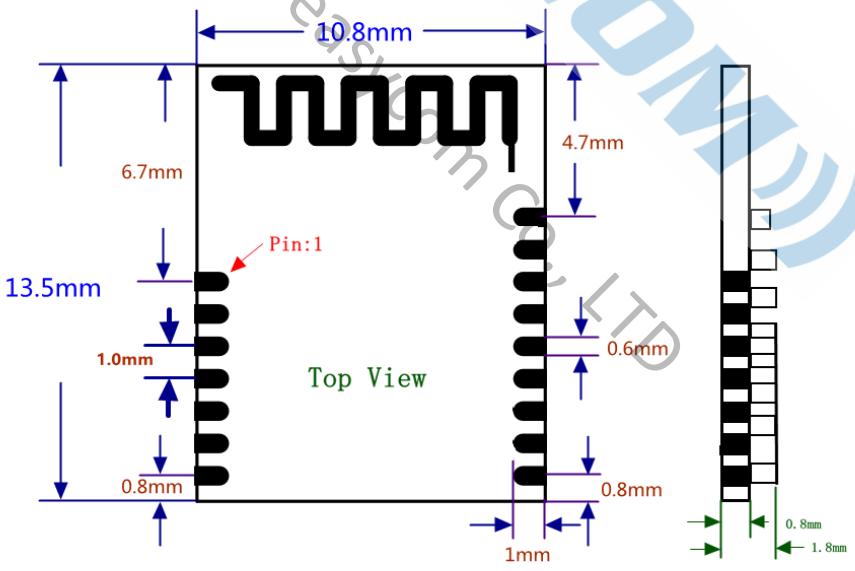

Figure 3: Pin Configuration and Package Dimensions（TOP VIEW）

4. PIN DEFINITION DESCRIPTIONS

Pin	Pin Name	Pad Type	Description
1	GND	VSS	Power Ground
2	PCM-CLK	Bi-directional	Synchronous data clock(operating votage level: 3.3V)
3	PCM_OUT	CMOS output	Synchronous data output(operating votage level: 3.3V)
4	PCM_IN	CMOS input	Synchronous data input(operating votage level: 3.3V)
5	PCM-SYNC	Bi-directional	Synchronous data sync(operating votage level: 3.3V)
6	NC	NC	
7	GND	VSS	Power Ground
8	GND	VSS	Power Ground
9	VDD_3V3	VDD	Power supply voltage 3.3V
10	BT_Enable	CMOS input	Module enable input(active high) **Note:** VDD_3V3 must be stable before pulling up BT_Enable
11	UART_RX	CMOS input	UART data input
12	UART_TX	CMOS output	UART data output
13	UART_RTS	CMOS output	UART request to send active low
14	UART_CTS	CMOS input	UART clear to send active low
15	GND	VSS	Power Ground
16	RF	RF_IN/OUT	Bluetooth 50ohm transmitter output/receiver input NC if using internal antenna(default) Connect to external antenna(optional)

Table 2

5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT825B is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT825B module	Data from FSC-BT825B module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT825B module	Request to send output of FSC-BT825B module
UART-CTS	Host	Clear to send input of FSC-BT825B module

Table 3

Default Data Format

Property	Possible Values
Baudrate	115. 2 Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 4

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%

Desired Baud Rate	Actual Baud Rate	Error (%)
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

Table 5. UART Interface Power-On Timing Parameters

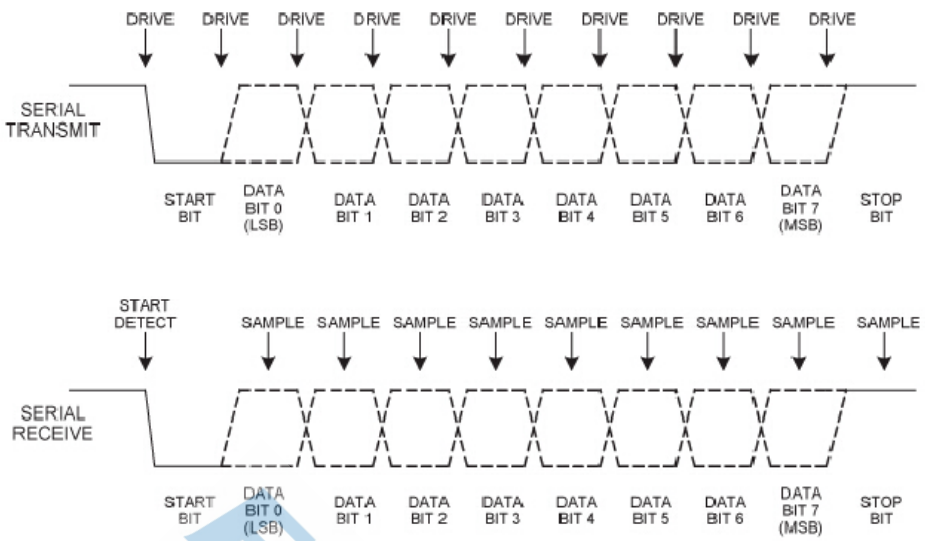

Figure 4: UART Interface Waveform PIN diagram

5.1.1 UART Interface Power-On Sequence

The UART interface power-on sequence differs depe nding on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

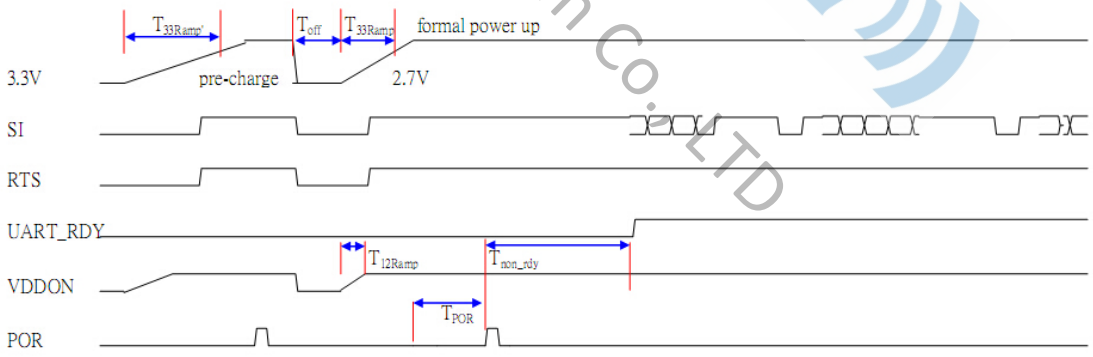

Figure 5: UART Power-On Sequence without Hardware Flow Control

UART Hardware Flow Control Supported

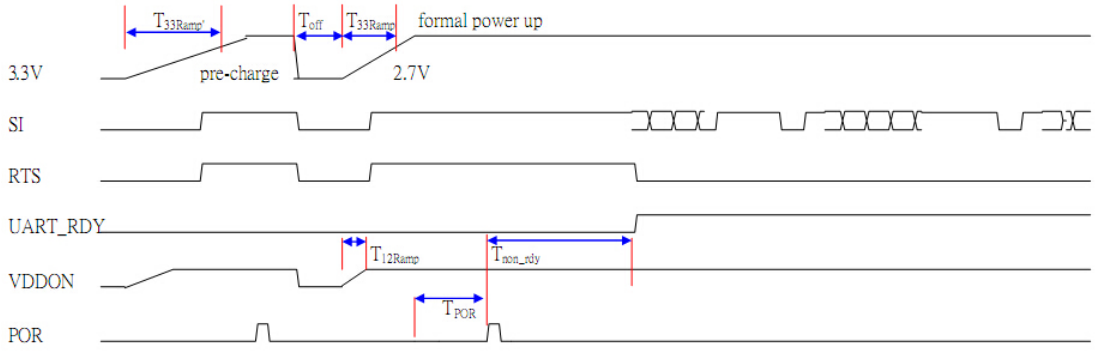

Figure 6: UART Power On Sequence with Hardware Flow Control

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the FSC-BT825B will not respond to any commands.

Table 6: UART Interface Power-On Sequence

In this state, the FSC-BT825B will not respond to any commands. divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the Toff period. The ramp up time is specified in the T33ramp duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enable s the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to waiting the Tnon_rdy time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

	Min	Tyupical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

Table 7: UART Interface Power On Timing Parameters

5.2 PCM CODEC Interface

The FSC-BT825B supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/u-law, and 13/16-bit linear PCM formats
- Supports Master and Slave mode
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports Master and Slave mode
- Supports SCO/ESCO link

5.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync, and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSnc.

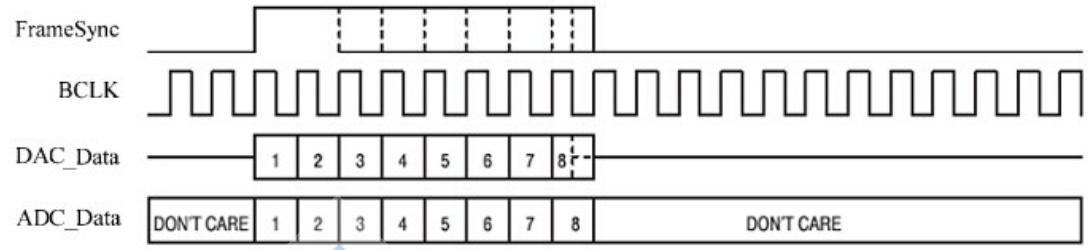

Figure 7. Long FrameSync

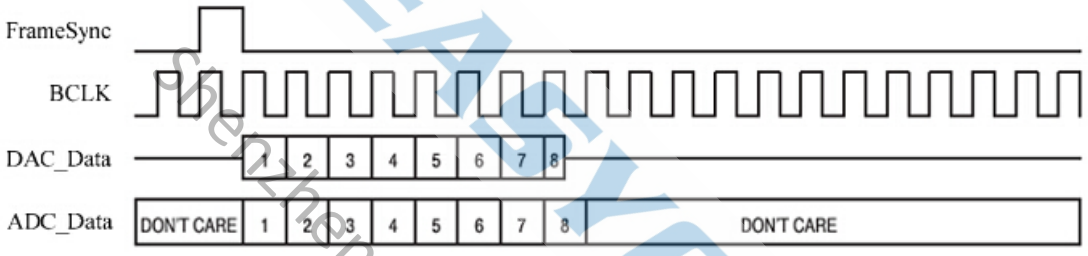

Figure 8. Short FrameSync

5.2.2 Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

◆For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

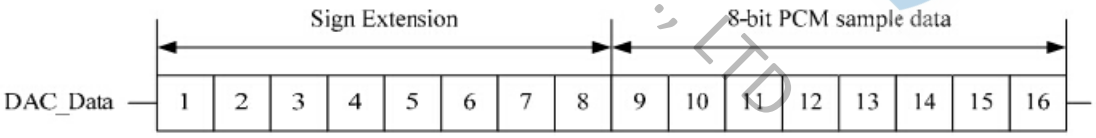

Figure 9. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

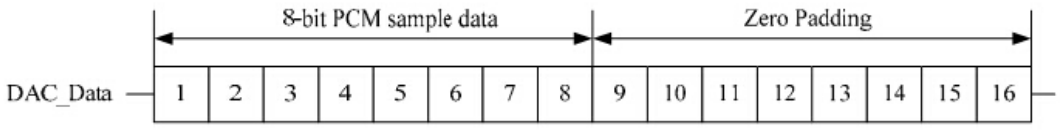

Figure 10 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

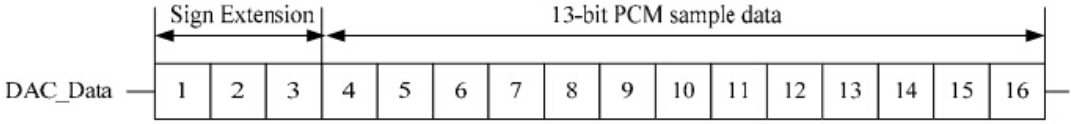

Figure 11. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

◆For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

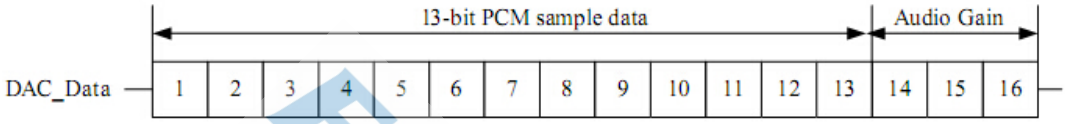

Figure 12. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

5.2.3 PCM Interface Timing

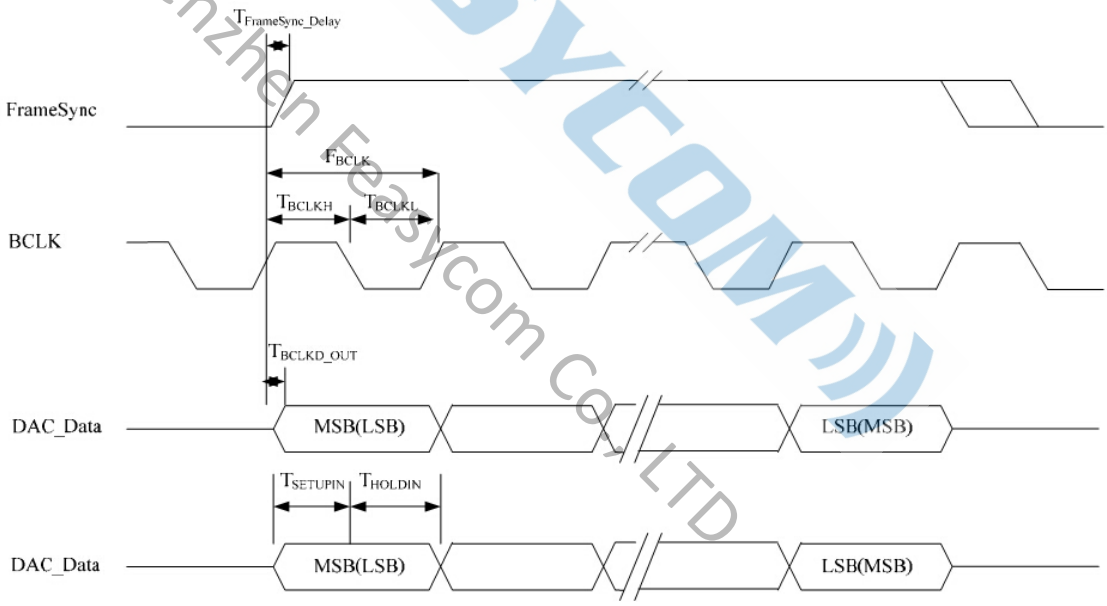

Figure 13: PCM Interface (Long FrameSync)

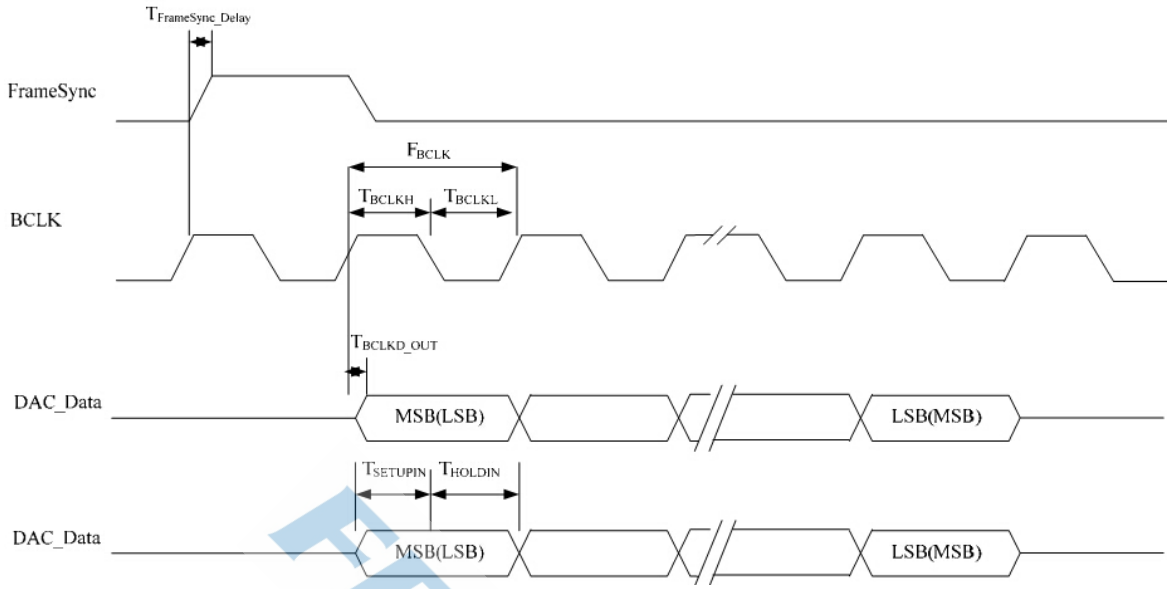

Figure 14: PCM Interface (Short FrameSync)

Symbol	Description	Min	Typ	Max	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	8	KHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	KHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 8: PCM Interface Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$F_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns

T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

Table 9: PCM Interface Timing

5.2.4 PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the FSC-BT825B PCM interface.

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30℃/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice (注意):

When using our modules, it is recommended to use a step steel mesh with a thickness of 0.16- 0.20mm. However, the thickness can be adjusted according to the adaptability of your own product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Table 10: Recommended baking times and temperatures

Feasycom surface mount modules are designed to simplify manufacturing processes, such as reflow soldering on a PCB. However, Customers are responsible for selecting the appropriate solder paste and confirming that the oven temperatures during reflow meet with the specifications provided by the solder paste manufacturer. Notably, Feasycom surface mount modules adhere to the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

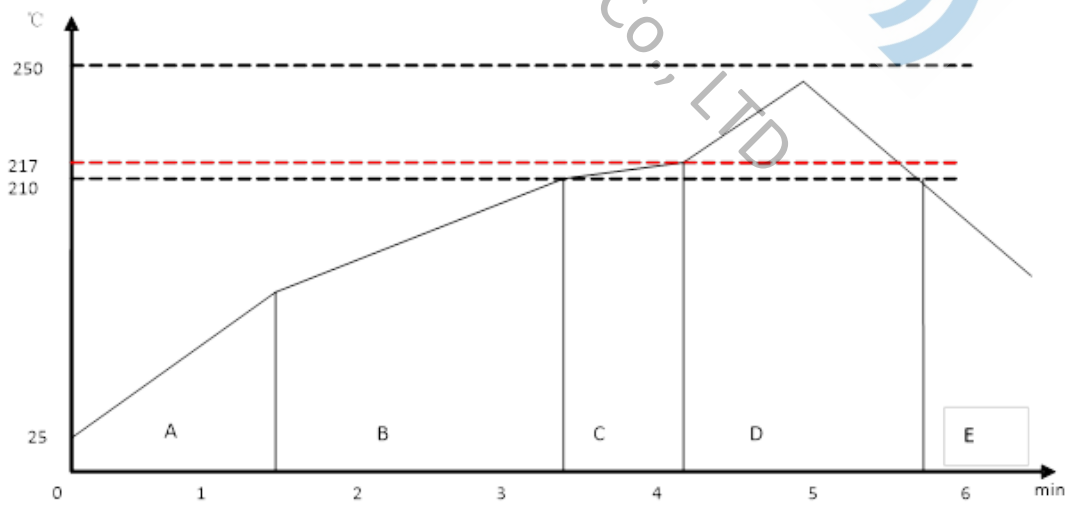

Figure 15: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate,

usually ranging from 0.5 to 2 °C/s. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the 0℃ space for 1 hour and then move to +70℃ space within 1minute, after 1 hour move back to 0℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT825B is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because

it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

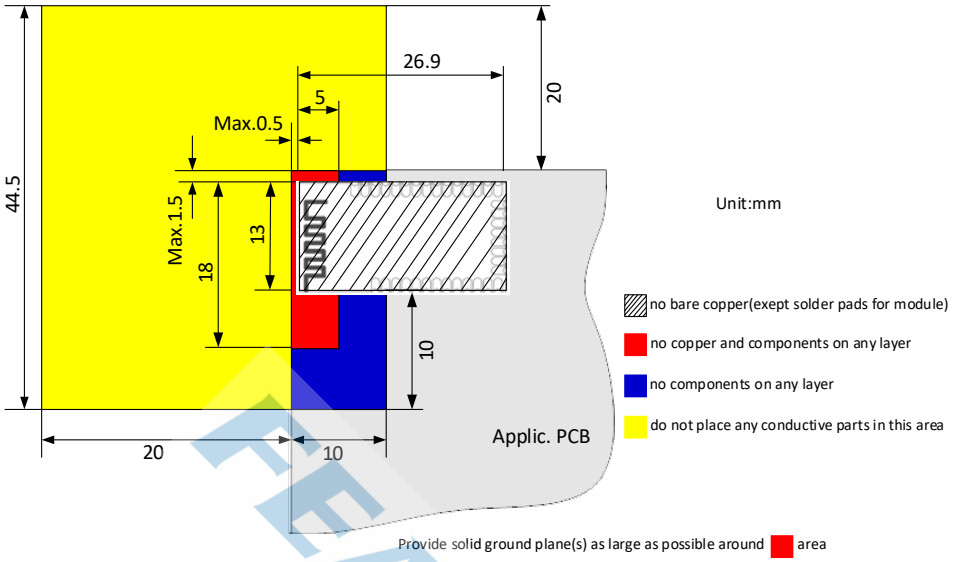

Figure 16: FSC-BT825B Restricted Area(Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9. Certificate

Has passed SRRC certification.

无线电发射设备
Radio Transmission Equipment
型号核准证
Type Approval Certificate

深圳市飞易通科技有限公司：

根据《中华人民共和国无线电管理条例》，经审查，下列无线电发射设备符合中华人民共和国无线电管理规定和技术标准，其核准代码为：CMIIT ID:2019DP8740

In accordance with the provisions on the Radio Regulations of the People's Republic of China, the following radio transmission equipment, after examination, conforms to the provisions with its CMIIT ID:

有效期：五年
Validity

（发证机关）
Sealed by issuing authority
2019年 9 月 11日
Year Month Date

编号：2019-8740
Number

设备名称：蓝牙模块
Equipment Name

设备型号：FSC-BT825B
Equipment Type

主要功能：数据传输
Main Functions

调制方式：GFSK π/4-DQPSK 8DPSK
Modulation Mode

主要技术参数及其指标值：
Main Technical Parameters

频率范围：2400-2483.5MHz
Frequency Range

频率容限：≤20ppm
Frequency Tolerance

发射功率：≤20dBm(EIRP)
Transmitting Power

占用带宽：≤2MHz
Occupied Bandwidth

杂散发射限值：≤-30dBm
Spurious Emission Limits

（核发单位章）
Sealed by issuing authority
2019年 9 月 11日
Year Month Date

10. Application Schematic