FSC-BT9101AI

DATASHEET V1.2

Revision History

Version	Data	Notes	Author
V1.0	2024-07-31	Initial Version	Liu
V1.1	2024-12-02	1, Change the Supply Voltage 2, Update Pin5-8 SPI interface，change Pin9,10,29,30,34 definition 3, Update BT-RX sensitivity	Liu
V1.2	2025-01-04	1, Update TX POWER	Liu

Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District,Shenzhen,518100,China.

Tel: 86-755-27924639

1 INTRODUCTION

Overview

FSC-BT9101AI supports Bluetooth dual-mode V5.3(BR/EDR/BLE).

By default, the FSC-BT9101AI module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over a serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT9101AI provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- **Supporting feature**:
  - Standard configurable RF transmission power -20 dBm to 0 dBm(±2dBm)
  - Low Power
  - Supports 1 Mbps/2 Mbps/3 Mbps BR/EDR
  - Supports 1 Mbps/2 Mbps LE
  - Supports long-distance transmission of LE 125Kbps/500Kbps
  - RSSI is supported
  - Dynamic TX power control
  - Bluetooth host protocol stack implemented by another MCU or host AP
- **RF Specification**:
  - RX Receiving sensitivity -88dBm (BR 1Mbps)
  - RX Receiving sensitivity -90dBm (EDR 2Mbps)
  - RX Receive sensitivity -82dBm (EDR 3Mbps)
  - RX Receive sensitivity -93dBm (LE 1Mbps)
  - RX Receiving sensitivity -90dBm (LE 2Mbps)
  - RX Receiving sensitivity -95dBm (LE LR2 1Mbps)
  - RX Receiving sensitivity -97dBm (LE LR8 1Mbps)
  - TX Transmit power -20 dBm to 0 dBm(±2dBm)

Applications

- Bluetooth KEY
- OBU
- Smart home
- data transmission module
- Dual-mode Bluetooth HCI controller
- High security and reliability of Bluetooth MCU applications

2 General Specifications

Table 2-1： General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth V5.3
	Frequency Band	2402MHz ~ 2480MHz
	Interface	UART/PIO/ADC
	Transmit Power	0 dBm
	Receiver	-90dBm（EDR 2Mbps）
Size		26.9 mm × 13 mm × 2.2 mm
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Supply Voltage		3.3V~3.6V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V, Charge device model: Pass ±500 V,

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

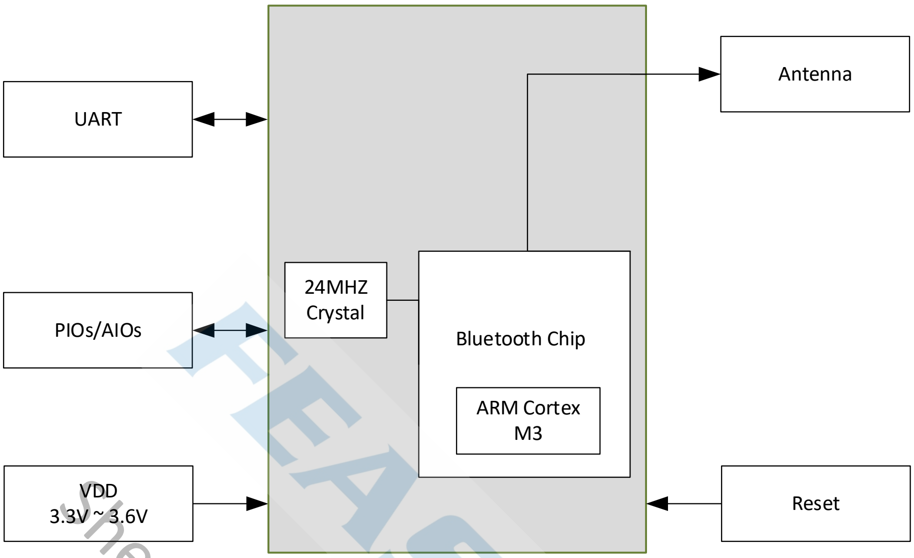


Figure 3-1-1: FSC-BT9101AI Block Diagram

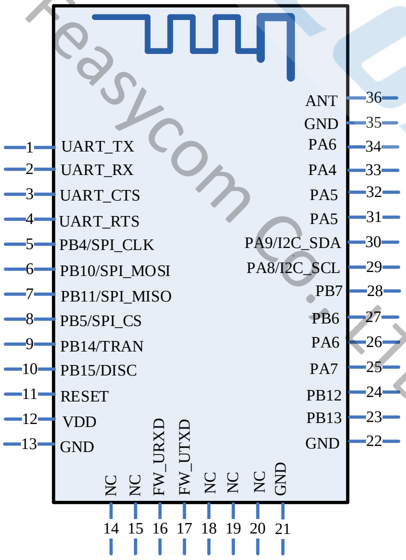


Figure 3-1-2: FSC-BT9101AI PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 3-2： Pin definitions

Pin	Pin Name	Type	Pin Descriptions
1	UART_TX	I/O	UART Data output
2	UART_RX	I/O	UART Data input
3	UART_CTS	I/O	UART Clear to Send (active low)
4	UART_RTS	I/O	UART Request to Send (active low)
5	PB4/SPI_CLK	I/O	Programmable input/output line Alternative Function 1: SPI_CLK (Default) **Alternative Function 2: NC (If the module has built-in SPI-flash)**
6	PB10/SPI_MOSI	I/O	Programmable input/output line Alternative Function 1: SPI_MOSI (Default) **Alternative Function 2: NC (If the module has built-in SPI-flash)**
7	PB11/SPI_MISO	I/O	Programmable input/output line Alternative Function 1: SPI_MISO (Default) **Alternative Function 2: NC (If the module has built-in SPI-flash)**
8	PB5/SPI_CS	I/O	Programmable input/output line Alternative Function 1: SPI_CS (Default) **Alternative Function 2: NC (If the module has built-in SPI-flash)**
9	PB14/TRAN	I/O	Host MCU change UART transmission mode. (Default) ***H = instruction mode*** ***L = throughput mode*** Alternative Function: Programmable input/output line
10	PB15/DISC	I/O	Host MCU disconnect bluetooth. (Default) Alternative Function: Programmable input/output line
11	RESET	I	External reset input: Active LOW. Set this pin low reset to initial state
12	VDD	Vdd	Power supply voltage 3.3V~ 3.6V
13	GND	Vss	Power Ground
14	NC	NC	
15	FW_URXD	I/O	Firmware download RXD
16	FW_UTXD	I/O	Firmware download TXD
17	NC	NC	
18	NC	NC	
19	NC	NC	
20	NC	NC	
21	GND	Vss	Power Ground
22	GND	Vss	Power Ground
23	PB13	I/O	Programmable input/output line

24	PB12	I/O	Programmable input/output line
25	PA7	I/O	Programmable input/output line
26/34	PA6	I/O	Programmable input/output line
27	PB6	I/O	Programmable input/output line
28	PB7	I/O	Programmable input/output line
29	PA8/I2C_SCL	I/O	Programmable input/output line **Alternative Function 1: I2C_SCL**
30	PA9/I2C_SDA	I/O	Programmable input/output line **Alternative Function 1: I2C_SDA** Alternative Function 2: BT Status
31/32	PA5	I/O	Programmable input/output line **Alternative Function 1: LED** **Power On: Light Slow Shinning; Connected: Steady Lighting.**
33	PA4	I/O	Programmable input/output line **Alternative Function 1: BT Status** ***Connected: High; Not connected: low.***
35	GND	Vss	Power Ground
36	EXT_ANT	O	RF signal output . If you need to use an external antenna, you can shield the onboard antenna by modifying the module on the 0R resistor. Or contact Feasycom to modify.

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT9101AI UART interface is a standard 4-wire interface with RX and TX. Supports H4 HCI interface or raw UART to application. The default baud rate is 115.2k baud. In order to support both high and low-speed baud rates, FSC-BT9101AI provides multiple UART clocks.

Table 4-1： Possible UART Settings

Parameter	Possible Values
Baudrate	Standard 115200bps
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5 MSL & ESD

Table 5-1: MSL and ESD

Parameter	Value
MSL grade	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

6 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30˚C/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice (注意):

When using our modules, it is recommended to use a step steel mesh with a thickness of 0.16-0.20mm. However, the thickness can be adjusted according to the adaptability of your own product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 6-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to simplify manufacturing processes, such as reflow soldering on a PCB. However, customers are responsible for selecting the appropriate solder paste and confirming that the oven temperatures during reflow meet with the specifications provided by the solder paste manufacturer. Notably, Feasycom surface mount modules adhere to the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is intended only as a general guideline for solder reflow and should be used as a reference.

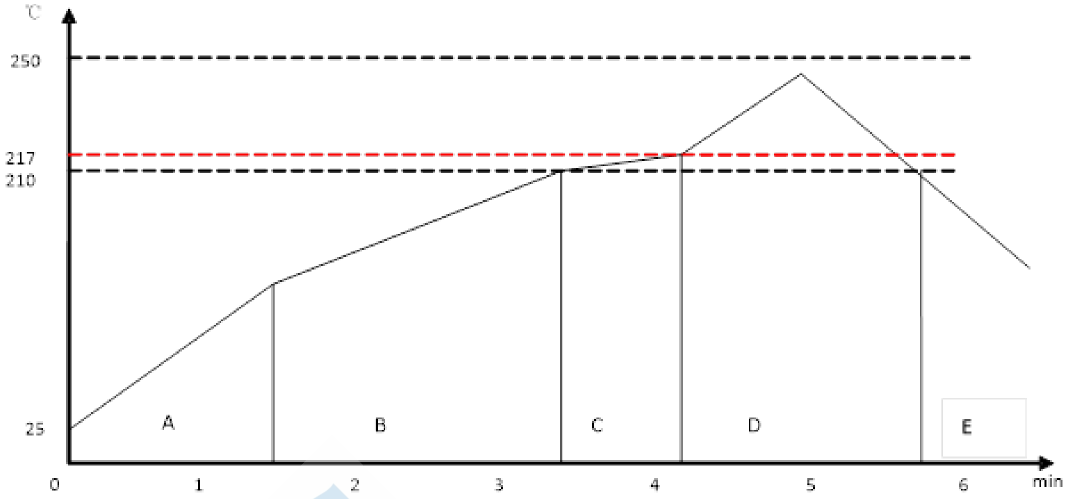


Figure6-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate, usually **ranging from 0.5 to 2 °C/s**. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component becomes activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. **For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.**

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solders. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

7 MECHANICAL DETAILS

7.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

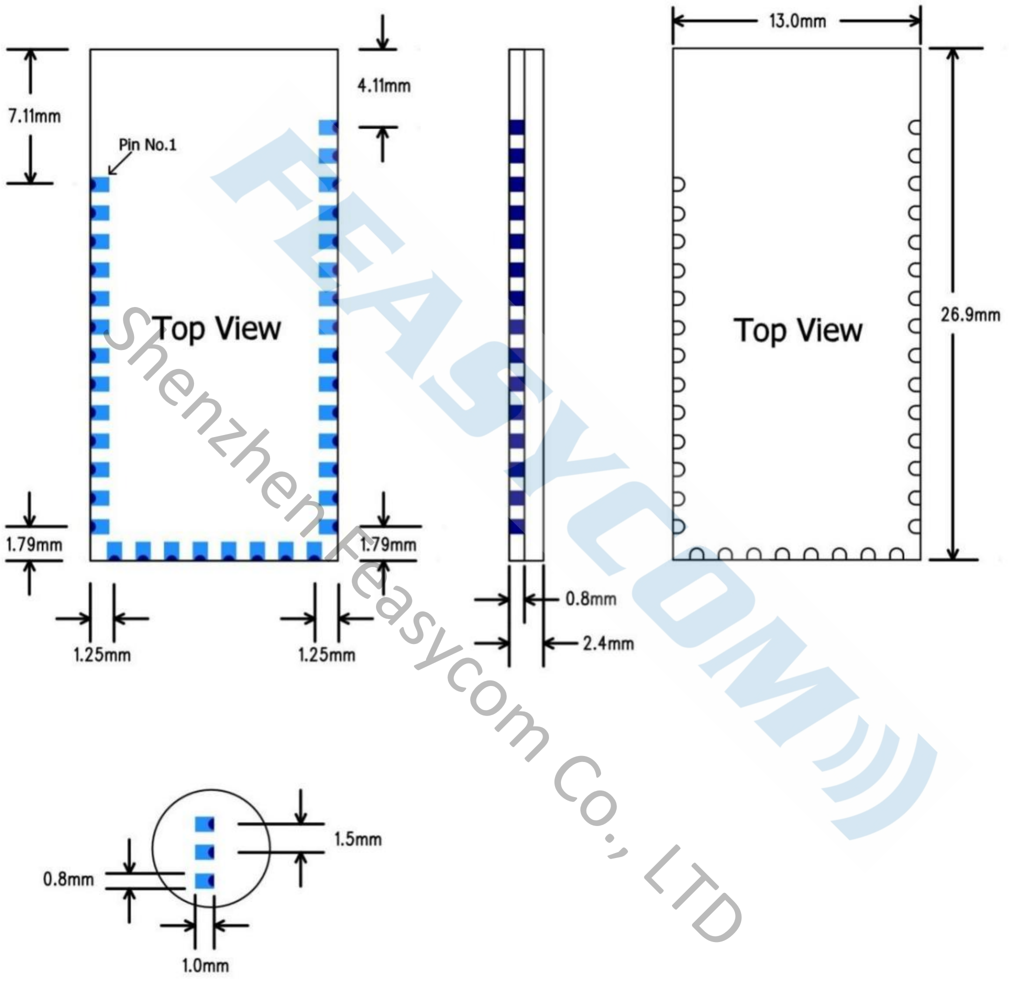


Figure 7-1： FSC-BT9101AI footprint Layout Guide (Top View)

8 HARDWARE INTEGRATION SUGGESTIONS

8.1 Soldering Recommendations

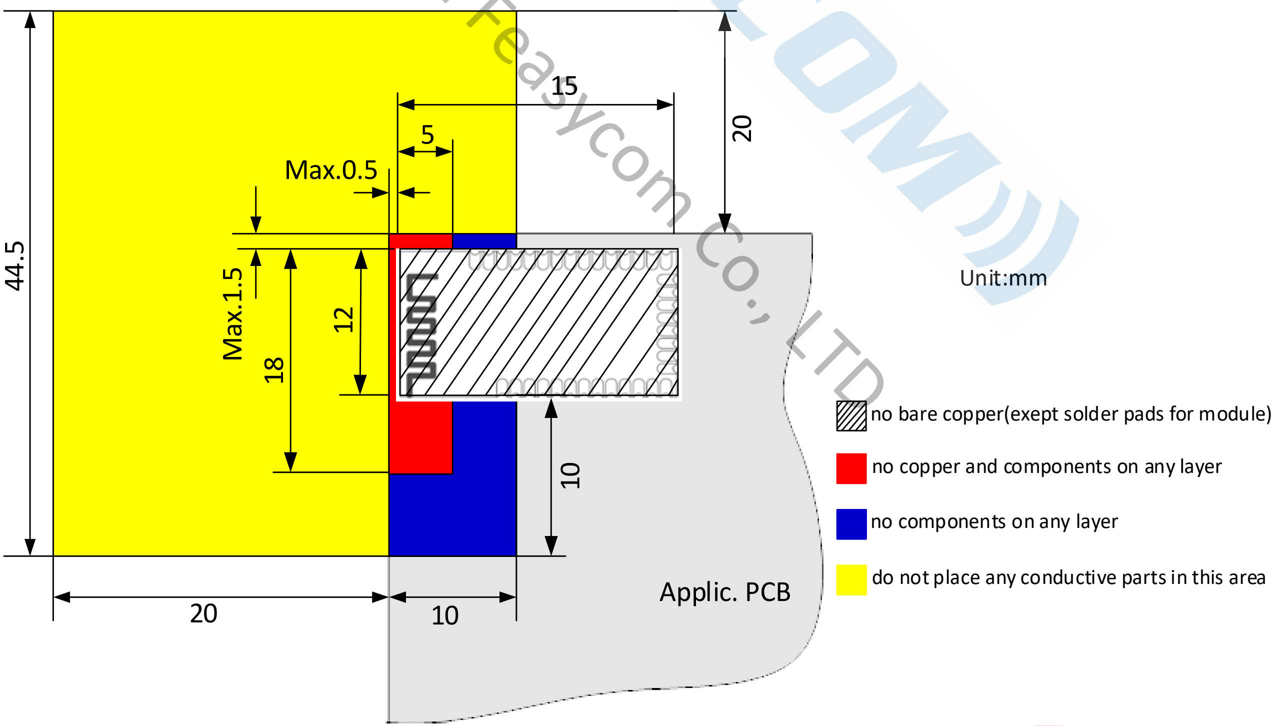
FSC-BT9101AI is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

8.2 Layout Guidelines (Internal Antenna)

It is strongly recommended to follow good layout practices in order to ensure proper operation of the module. Placing copper or any metal near the antenna can negatively impact its performance by affecting the matching properties. To prevent radiation, a metal shield should not be used with the module. It is advised to use grounding vias, spaced a maximum of 3 mm apart, at the edge of grounding areas to prevent RF penetration inside the PCB and unintentional resonator formation. Additionally, GND vias should be distributed all around the PCB edges.

In the restricted area where the on-board antenna is located, the motherboard should not have any bare conductors or vias. This area is not covered by stop mask print, so no copper (planes, traces, or vias) should be present in this area to avoid mismatching with the on-board antenna.



Provide solid ground plane(s) as large as possible around 🟥 area

Figure 8-2：Restricted Area (Design schematic, for reference only. Unit: mm)

The following recommendations aim to avoid EMC problems caused by the RF portion of the module. It is important to note that each design is unique, and this list does not cover all basic design rules, such as avoiding capacitive coupling between signal lines. Additionally, it is crucial to consider potential problems arising from digital signals in the design.

To mitigate EMC issues, it is advisable to ensure that signal lines have return paths that are as short as possible. For instance, if a signal passes through a via to an inner layer, always use ground vias around it. These ground vias should be located tightly and symmetrically around the signal vias. Routing of sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area both above and below the line. If this is not feasible, make sure to keep the return path short by employing alternative methods, such as placing a ground line next to the signal line.

8.3 Layout Guidelines (External Antenna)

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antennas designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the system PCB.

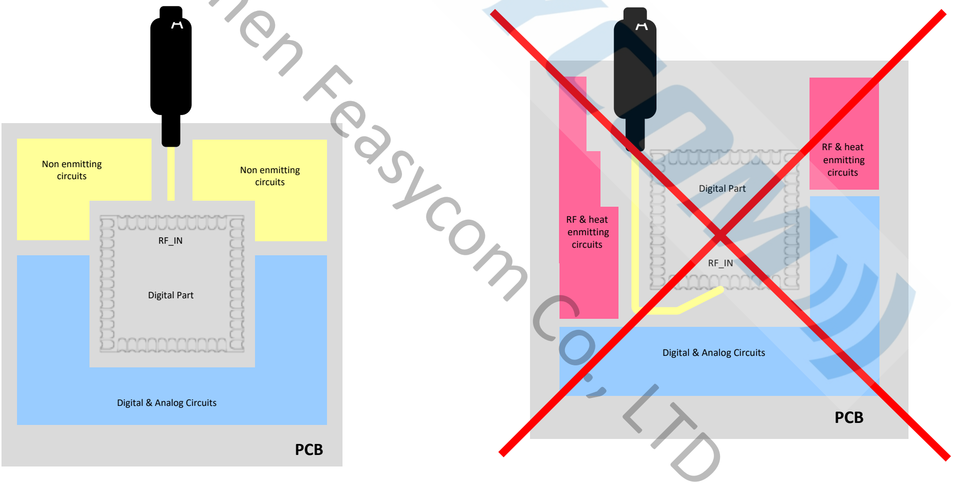


Figure 8-3: Placement the Module on a System Board

8.3.1 Antenna Connection and Grounding Plane Design

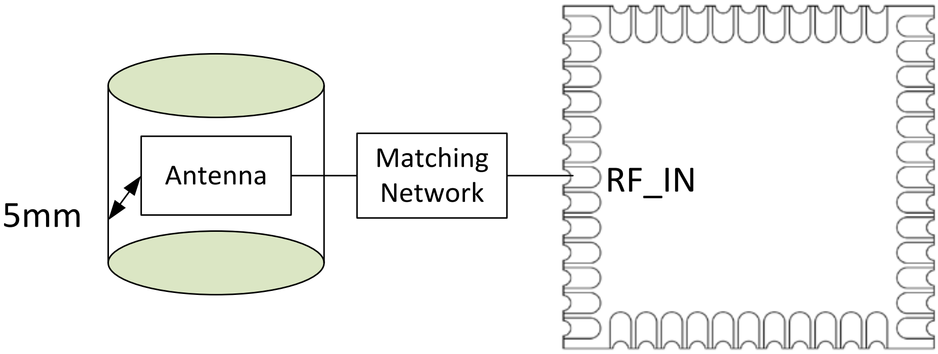


Figure 8-3-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

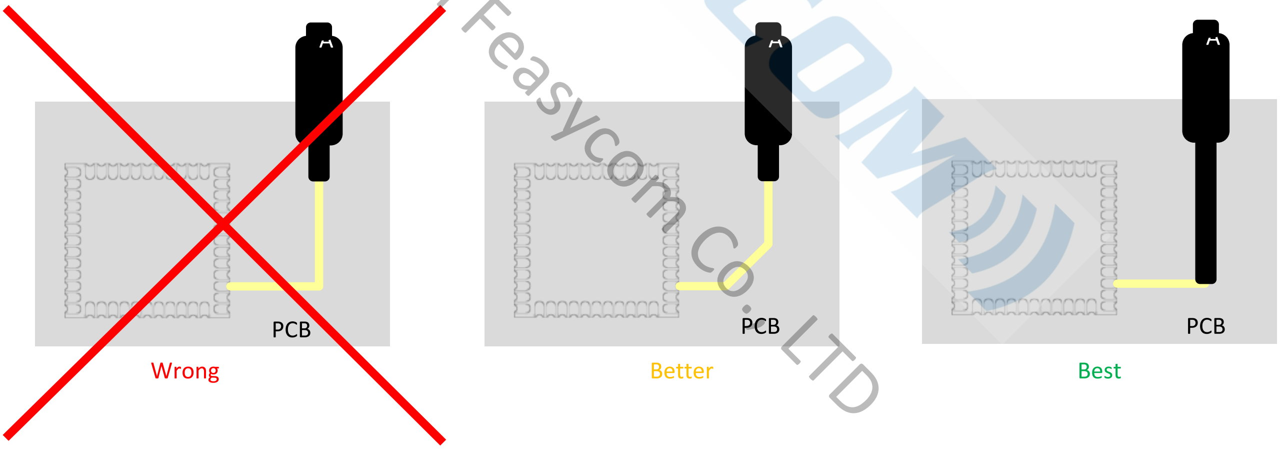


Figure 8-3-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use multiple vias as possible to connect the ground planes.

9 PRODUCT PACKAGING INFORMATION

9.1 Default Packing

Figure 9-1: Tray Dimension: 140mm * 265mm Tray vacuum

9.2 Packing box (Optional)

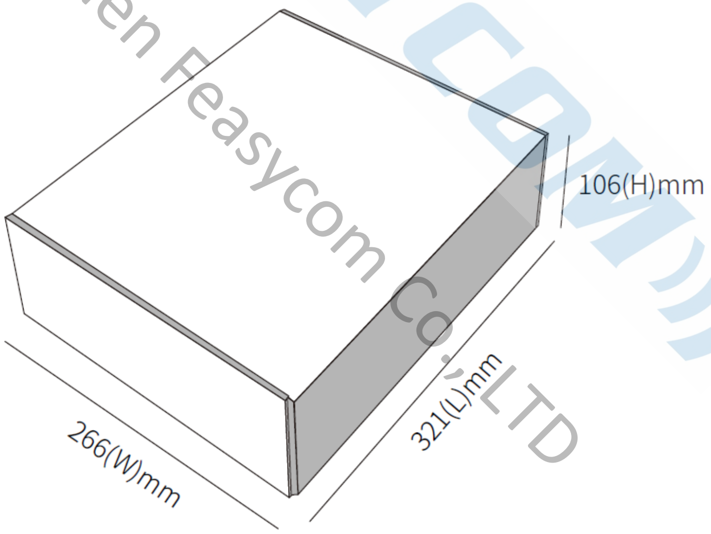


Figure 9-2: Packing box (Optional)

** If any packaging other than the package mentioned above is required, please confirm the packaging size again.*

** Packing: 1000pcs per carton (Minimum packing quantity).*

** The outer packing size provided above is for reference purposes only. For the actual dimensions of the product's packaging, please refer to the packaging of the actual goods.*

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10 APPLICATION SCHEMATIC