FSC-BW105

Bluetooth 5.0 + Dual-band 2x2 802.11ac Module Datasheet

Version 1.1

Revision History

Version	Data	Notes	Approved By
1.0	2021/07/10	Initial Version	Marsh
1.1	2022/08/05	1. Add the module picture, modify the description, 2. Add the application circuit diagram	Devin Wan

Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District, Shenzhen, 518102, China
Tel: 86-755-27924639

Contents

1. INTRODUCTION

Overview

FSC-BW105 uses the gauge level IC QCA6574A，it is a single-die wireless local area network (WLAN) and Bluetooth (BT) combo solution to support 2x2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards and BT 5.0 enabling seamless integration of WLAN/BT and Low Energy technology.

FSC-BW105 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. As a result, enhanced overall quality for simultaneous voice, video, and transmission is achieved.

FSC-BW105 is an appropriate product for designers who want to add wireless capability to their products. Let all of the system high design flexibility, short development cycle, and quick time-to-market.

General Features

- Highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 5 GHz 802.11ac, or 2.4/5GHz 802.11n WLAN applications
- Supports BT 5.0, ANT+ and is backward-compatible with previous BT versions from v1.2
- Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Rx Space Time Block Code (STBC)
- Supports 20/40 MHz at 2.4 GHz and supports 20/40/80MHz at 5 GHz
- Supports BT-WLAN coexistence and ISM-LTE coexistence
- Support BT for class 1 and class 2 power-level transmissions without requiring an external PA (power amplifier)
- Enhanced qualification based on selective AEC Q100 and JEDEC test cases
- Single-stream spatial multiplexing up to 433.3 Mbps data rate. (Under dual-antenna status, 802.11ac:Up to 867Mbps)
- PCIe interface for WLAN and UART/PCM interface for BT
- UART(Max Baud Rate 3.2Mbps)
- Stamp module suitable for Surface Mounted Technology (SMT)
- Iron Shielding case
- Stamp-64 package
- Dimension(Iron Shielding Case) : 22mm(L) x 22mm(W) x 2.4mm(H)
- Operating Voltage :
  VBAT : 3.14 to 3.46V ; VIO: 1.71 to 3.46V
- RoHS / REACH Compliant
- External Antenna
- BT profiles: HFP, A2DP, AVRCP, PBAP, SPP, GATT, HID, DUN, FTP, ANCS
- Support Android /Linux

Application

- Car audio and video system
- Measurement systems
- STB/OTT/IPTV

Module picture as below showing

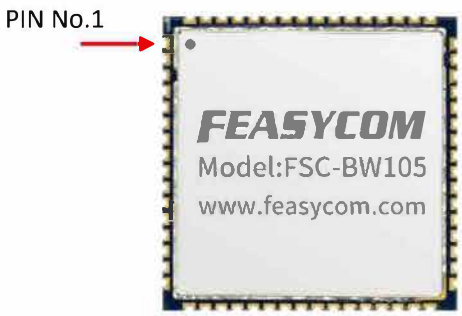


Figure 1: FSC-BW105 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.0+EDR
Frequency Band		2402MHz~2480MHz
Bluetooth class		Class 1 and Class 2
Range, line of sight		Up to 10m for audio, up to 50m for data
Transmit power		9dBm Max
Receiver sensitivity		-89dBm
Support mode		Slave and Master
Profiles		HFP, A2DP, AVRCP, SPP, PBAP, HID, DUN, FTP, GATT, ANCS
Maximum throughput		3Mbps
Interface		UART/PCM
WIFI		
Wi-Fi standard		2.4G: IEEE802.11 b/g/n radio 5G: IEEE802.11 a/n/ac radio
Range, line of sight		Up to 100m
Frequency Band		2.4GHz and 5GHz frequency band
Transmit power		17dBm(Maximum) 10dBm(Minimum)
Receiver sensitivity		-80dBm@11Mbps -71dBm@54Mbps -70dBm@HT20 MCS7 -70dBm@HT40 MCS7 -60dBm@VHT80 MCS9
Mode		WIFI-AP(access point), WIFI-Station
Maximum throughput		802.11b:Up to 11Mbps 802.11g:Up to 54Mbps 802.11n:Up to 300Mbps 802.11ac:Up to 867Mbps(Under dual-antenna status)
Security		WEP, TKIP, AES, WPA, WPA2
Interface		PCIe
General		
Size		22mm(L) x 22mm(W) x 2.4mm(H)
Hardware Interface		UART, GPIO, PCIe, PCM/I2S
Antenna		External (Dual-band antenna, supporting 2.4GHz and 5.8GHz frequencies)
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Operating voltage (VBAT)		3.14 to 3.46V
VIO		1.71 to 3.46V

Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±250 V, all pins

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

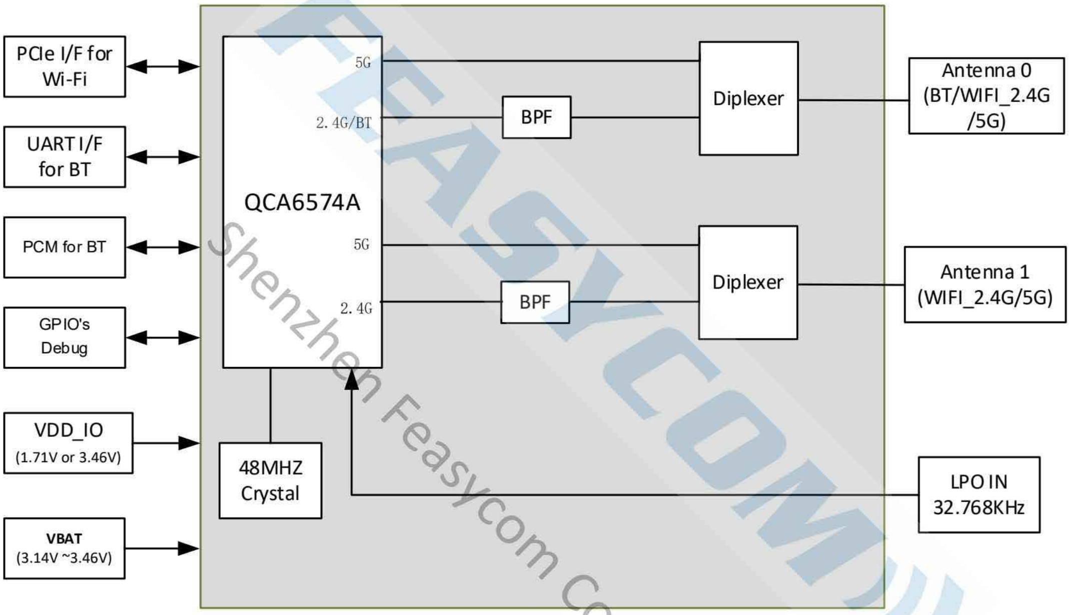


Figure 2: Block Diagram

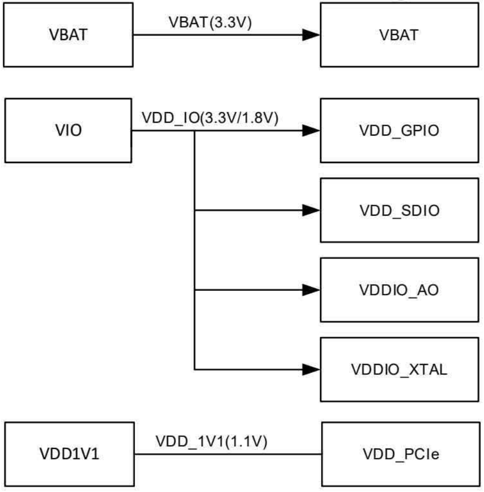


Figure 3: Block diagram of the power section

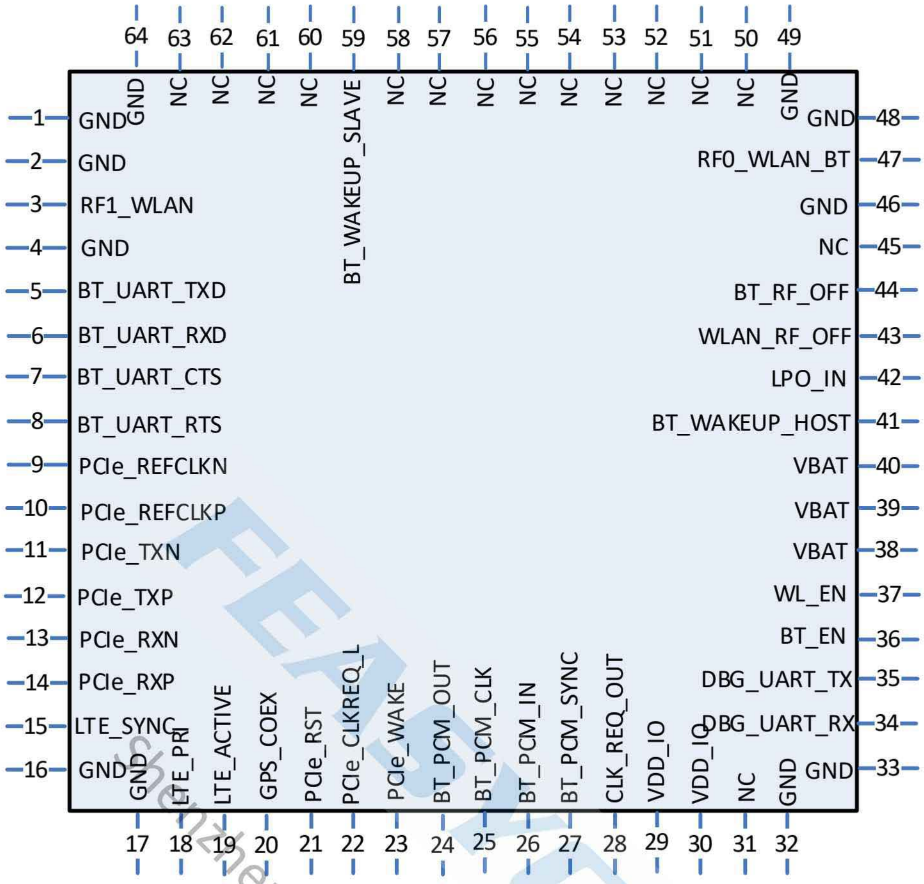


Figure 4: FSC-BW105 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	VSS	Ground	
2	GND	VSS	Ground	
3	RF1_BT/WLAN	RF	WLAN 2.4/5GHz and RF input/output port for chain 1	
4	GND	VSS	Ground	
5	BT_UART_TXD	O	BT UART serial output	
6	BT_UART_RXD	I	BT UART serial input	
7	BT_UART_CTS	I/O	BT UART clear-to-send	
8	BT_UART_RTS	I/O	BT UART request-to-send	
9	PCIe_CLKN	I	PCI Express Differential Reference. Clock Source:100MHz	
10	PCIe_CLKP	I		
11	PCIe_TXN	O	PCI Express Transmit Differential Pair	
12	PCIe_TXP	O	PCI Express Transmit Differential Pair	
13	PCIe_RXN	I	PCI Express Receive Differential Pair	
14	PCIe_RXP	I	PCI Express Receive Differential Pair	
15	LTE_SYNC	I	LTE co-existence signal. LTE_UART_RXD or LTE_FS	
16	GND	VSS	Ground	
17	GND	VSS	Ground	

18	LTE_PRI	O	LTE co-existence signal. LTE_UART_TXD or LTE_PRI
19	LTE_ACTIVE	I	LTE co-existence signal.(it is not required if using 2-wire interface for LTE-coexistence
20	GPS_COEX	I	GPS co-existence signal. High means WLAN is in transmit. NC if not used.
21	PCIe_RST	I	PCI express reset with weak pull-down
22	PCIe_CLKREQ_L	O	Reference clock request(the pin must be 3.3V; VDD_IO input to 1.8V or 3.3V)
23	PCIE_WAKE	O	Request to service a function-initiated wake event
24	BT_PCM_OUT	O	BT PCM output signal
25	BT_PCM_CLK	I/O	BT PCM clock signal
26	BT_PCM_IN	I	BT PCM input signal
27	BT_PCM_SYNC	I/O	BT PCM synchronization signal
28	CLK_REQ_OUT	O	Clock Request Output
29	VDD_IO	I/O	1.8Vor 3.3V(Input); Connect to 1.8V or 3.3V external power
30	VDD_IO	I/O	1.8Vor 3.3V(Input); Connect to 1.8V or 3.3V external power
31	NC	-	Not Connected
32	GND	VSS	Ground
33	GND	VSS	Ground
34	DBG_UART_RX	I	WLAN Debug Signal(Reserved Point)
35	DBG_UART_TX	O	WLAN Debug Signal(Reserved Point)
36	BT_EN	I	Bluetooth Function Enable(the pin must be 3.3V; VDD_IO input to 1.8V or 3.3V)
37	WL_EN	I	Wi-Fi Function Enable(the pin must be 3.3V; VDD_IO input to 1.8V or 3.3V)
38	VBAT	PWR	Module Main Power Input (3.3V)
39	VBAT	PWR	Module Main Power Input (3.3V)
40	VBAT	PWR	Module Main Power Input (3.3V)
41	BT_WAKEUP_HOST	O	Bluetooth wakeup the host, active high
42	LPO_IN	I	External low-power clock input(32.768kHz)
43	WLAN_RF_OFF	I	Turn-off WLAN RF analog and front-end. Active low
44	BT_RF_OFF	I	Turn-off Bluetooth RF analog and front-end. Active low
45	NC	I	External low-power 32.768 kHz clock input.
46	GND	VSS	Ground
47	RF0_ WLAN_BT	RF	WLAN 2.4/5GHz and Bluetooth RF input/output port chain 0
48	GND	VSS	Ground
49	GND	VSS	Ground
50	NC	-	Not Connected
51	NC	-	Not Connected
52	NC	-	Not Connected
53	NC	-	Not Connected
54	NC	-	Not Connected
55	NC	-	Not Connected
56	NC	-	Not Connected

57	NC	-	Not Connected
58	NC	-	Not Connected
59	BT_WAKEUP_SLAVE	I	Host wakeup Bluetooth, active high
60	NC	-	Not Connected
61	NC	-	Not Connected
62	NC	-	Not Connected
63	NC	-	Not Connected
64	GND	VSS	Ground

4. PHYSICAL INTERFACE

4.1 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 3.2 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbps.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

FSC-BW105 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

FSC-BW105 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	9600 baud (≤0%Error)
	Standard	115200bps(≤1.6%Error)
	Maximum	3.2Mbps(≤0%Error)

Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

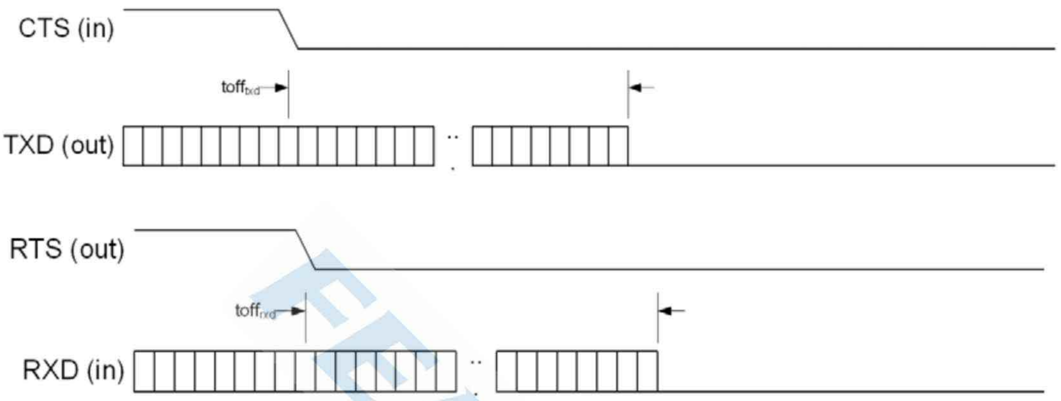


Figure 5: UART Timing

Table 4: UART Timing Specifications

Parameter	Description	Min	Type	Max	Unit
toff_{txd}	Delay from CTS to TXD stop	-	-	1	byte
toff_{rxd}	Delay from RTS to RXD stop	16	-	-	byte

4.2 Bluetooth PCM Interface

The pulse coded modulation (PCM) interface connects the FSC-BW105 to the phone’s audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDD_IO supply. Their I/O performance specifications meet the requirements stated.

FSC-BW105 PCM interface has been designed to minimize audio latency. The typical audio latencies for various packet types as follows.

Table 5: Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 Tesco=6,Wesco=0	4.4mS
EV3 Tesco=6,Wesco=2	5.7mS
EV3 Tesco=6,Wesco=4	6.9mS

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether FSC-BW105 PCM interface is configured as master or slave:

- When FSC-BW105 PCM interface is the master : PCM_CLK and PCM_SYNC are outputs from the device to the PCM bus slave(s).
- When FSC-BW105 PCM interface is the slave : PCM_CLK and PCM_SYNC are inputs to the device from the PCM bus master.

Table 6: PCM interface specifications

Parameter	Min	Type	Max	Unit
Clock rate(Slave)—Determined by the master	64	-	2048	KHz
Clock rate(Master)—(32MHz *N/4000),in which N is an integer	64	-	2048	KHz
Frame size	1	8	256	Bits
Slot size	1	13	16	Bits
Slot number—Number of slots that can be configured per frame	1	-	32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following tables and illustrations.

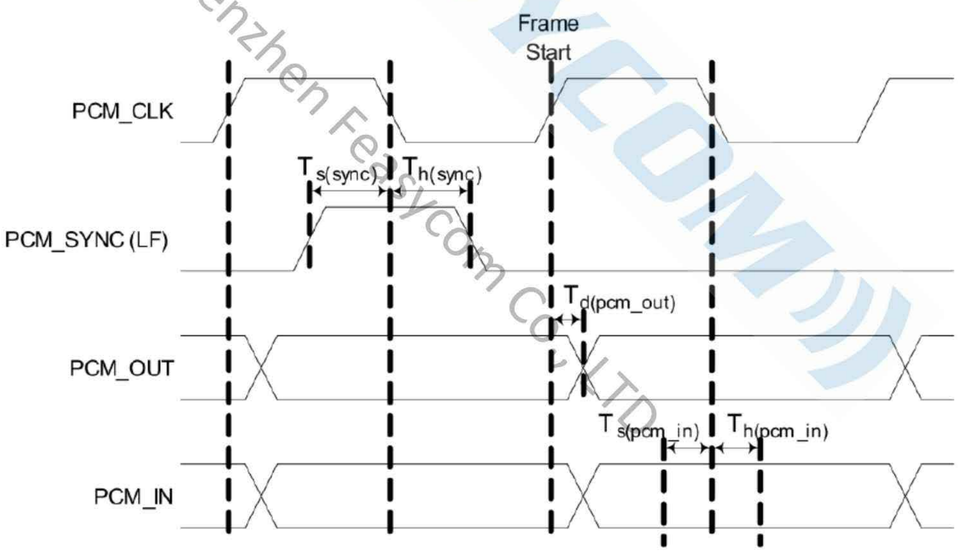


Figure 6: PCM interface timing diagram(slave)

Table 7: PCM interface timing in slave mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Setup time PCM_SYNC to PCM_CLK fall	0	-	-	ns
Hold time PCM_CLK fall to PCM_SYNC fall	150	-	-	ns
Delay from PCM_CLK rise to PCM_OUT	0	-	150	ns
Setup time PCM_IN to PCM_CLK fall	0	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

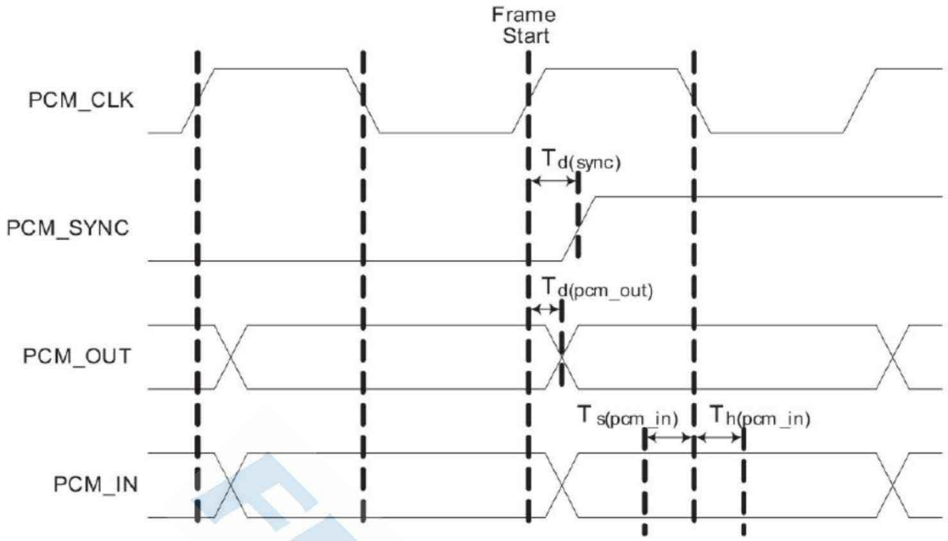


Figure 7: PCM interface timing diagram(master)

Table 8: PCM interface timing in master mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Delay from PCM_CLK rise to long SYNC	-10	-	50	ns
Delay from PCM_CLK rise to PCM_OUT	-10	-	50	ns
Setup time PCM_IN to PCM_CLK fall	50	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

4.3 PCI Express Interface

The PCI Express (PCIe) core on the FSC-BW105 is a high-performance serial I/O inter connect that is protocol compliant and electrically compatible with the PCI Express Base Specification v2.0. This core contains all the necessary blocks, including logical and electrical functional sub blocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)

Table 9: Absolute Maximum Rating

Parameter	Min	Max	Unit
VBAT(SWREG Supply Input)	-0.3	+3.6	V
VIO(DC supply voltage for digital I/O)	-0.3	+3.6	V
Operating temperature (T_A)	-40	+85	°C
Storage temperature (T_{stg})	-40	+85	°C
Maximum junction temperature(T_j)	-40	+115	°C
RF_{IN} Maximum RF input (reference to 50Ω input)		0	dBm

5.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VBAT	3.14	3.3	3.46	V
VIO	1.71	1.8~3.3	3.46	°C
Operating temperature (T_A)	-40	25	+85	°C
Storage temperature (T_{stg})	-40	25	+85	°C
High-level input voltage	0.7 X VIO		VDD_IO + 0.3	V
Low-level input voltage	-0.3		0.3 X VIO	V
Input low leakage current	-5.0		5.0	uA
High-level output voltage	0.9 X VIO		VIO	V
Low-level output voltage	0		0.1 X VIO	V
High-level output current	3			mA
Low-level output current			-11	mA
Input capacitance			3	pF

5.3 RF Characteristic

5.3.1 WLAN RF Characteristics(Transmitter)

Table 11: WLAN Transmitter

Characteristics	Condition	EVM	Min	Type	Max	Unit
2.4GHz						
Output Power	11M CCK		13	17	18	dBm
	6M OFDM		14	16	17	dBm
	54M OFDM	-25	11	15	16	dBm
	6.5M,MCS0(HT20)		12	15	17	dBm
	65M,MCS7(HT20)	-27	10	13	15	dBm
	6.5M,MCS0(HT40)		11	14	16	dBm
	65M,MCS7(HT40)	-27	10	13	15	dBm

	180M,MCS9(VHT40)	-32	8	10	13	dBm
5GHz						
Output Power	54M OFDM	-25	10	14	16	dBm
	65M,MCS7(HT20)	-27	8	13	16	dBm
	78M,MCS7(VHT20)	-30	8	13	16	dBm
	180M,MCS7(VHT40)	-32	8	11	16	dBm
	390M,MCS9(VHT80)	-32	6	10	12	dBm

5.3.2 WLAN RF Characteristics(Receive)

Table 12: WLAN Receive

Characteristics	Condition	Min	Type	Max	Unit
2.4GHz					
Sensitivity	11M CCK		-79	-80	dBm
	54M OFDM		-71	-72	dBm
	65M,MCS7(HT20)		-70	-71	dBm
5GHz					
Sensitivity	54M OFDM		-71	-74	dBm
	65M,MCS7(HT20)		-70	-72	dBm
	130M,MCS7(HT40)		-69	-71	dBm
	78M,MCS8(VHT20)		-59	-62	dBm
	180M,MCS9(VHT40)		-57	-61	dBm
	390M,MCS9(VHT80)		-56	-59	dBm

5.3.3 Bluetooth RF Characteristics

Table 13: Bluetooth RF Characteristics

Characteristics	Condition	Min	Type	Max	Unit
Bluetooth specification	Version 5.0				
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)				
BT Transmitter, GFSK					
RF output power			8.5	9	dBm
Power control step		2	4	8	dB
BT Receiver Characteristics, Basic rate receiver					
Sensitivity	GFSK, BER = 0.1%		-88		dBm
	Pi/4-DQPSK, BER = 0.01%		-89		dBm
	8DPSK, BER = 0.01%		-82		
Max. useable input power	GFSK, BER = 0.1%	-5			dBm

	Pi/4-DQPSK, BER = 0.1%	-10			dBm
	8DPSK, BER = 0.1%	-10			dBm

BLE RF Characteristics					
BLE Transmitter output power			4		dBm
BT Receiver Characteristics, Low energy receiver	BER <= 0.1%		-88	-90	dBm

5.4 Digital pad internal pull resistor

Table 14: Digital pad internal pull resistor

Internal Pull Resistor	VIO = 1.8V		VIO = 3.3V	
	R(KΩ)		R(KΩ)	
	Min	MAX	Min	MAX
Pull down	23	72	24	60
Pull up	70	168	49	95

5.5 Power Up/Down Sequence

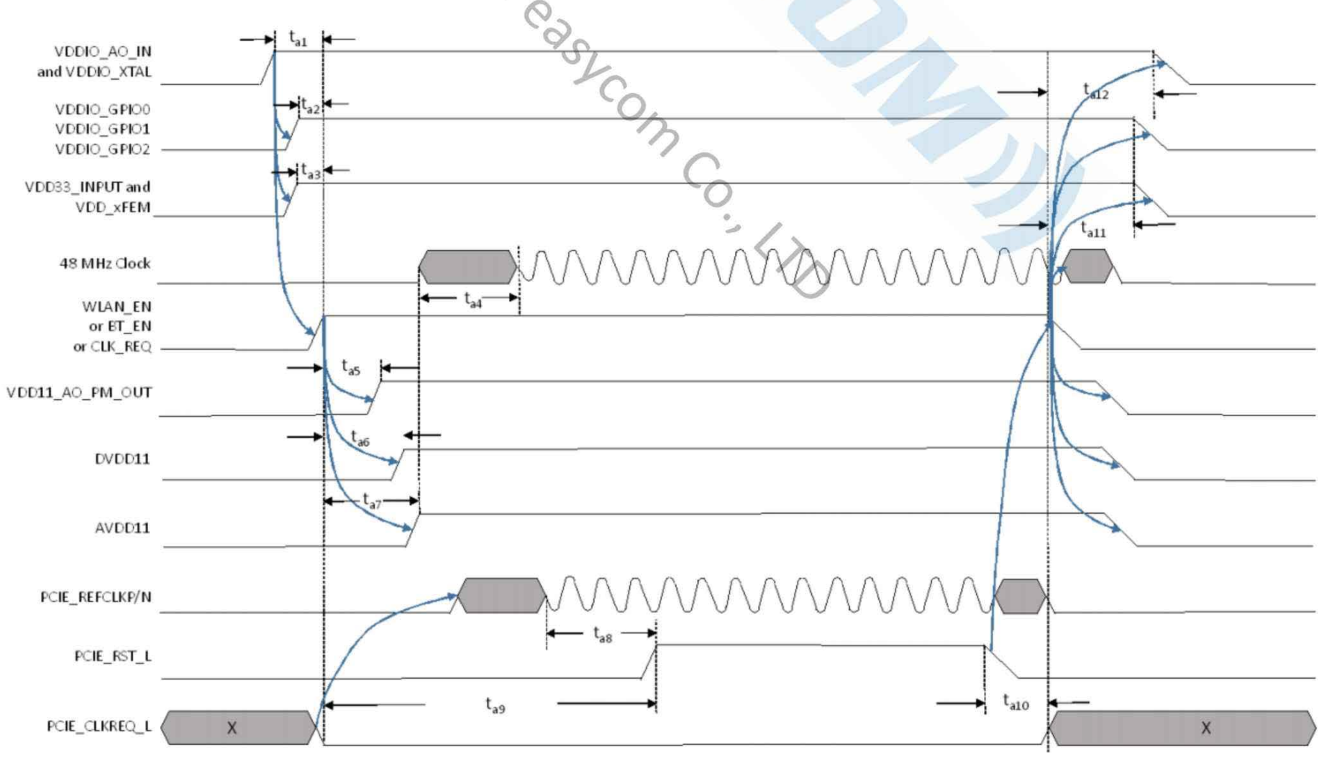


Figure 8: Power on and power off timing Sequence

Table 15: Power on and power off timing Sequence

Parameter	Min	Type	Max	Unit
ta1--VDDIO_AO valid to WL_EN input active (see note)	12			uS
ta2--VDDIO_XXX valid to WL_EN input active	10			uS
ta3--VDD33 valid to WL_EN input active	10			uS
ta4--48 MHz clock stabilization time	1			mS
ta5--WL_EN valid to AO 1.1 V established			500	uS
ta6--SDIO IO enable valid to DVDD11 established			2.5	mS
ta7--SDIO IO enable valid to AVDD11 established			3	mS
ta8--WL_EN valid to SDIO IO enable set by HOST	1			mS
ta9--SDIO IO enable valid to SDIO ready (including FW running time)			10	mS
ta10--SDIO CLK stable before SDIO IO enable set by HOST	400			uS
ta11--WL_EN de-assert to VDDIO_XXX and VDD33 ramping down	10			uS
ta12--WL_EN de-assert to VDDIO_AO ramping down (see note)	12			uS
NOTE:VDDIO_AO needs to be on at first and off at last, VDDIO_AO must be >1.62 V at all times when VDD33 > 1 V.				

5.6 Power Consumption

Table 16: Power Consumption:

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VBAT	3.3V	500
VIO	3.3V	300
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW105 Module Power Consumption:
500mA @ VBAT(Maximum) and 300mA @ VIO(Maximum)

Suggest customer design power capacity are 1000mA@VBAT and 500mA @ VIO for FSC-BW105 Module.

6. MSL & ESD

Table 17: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±250 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,

it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 18: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

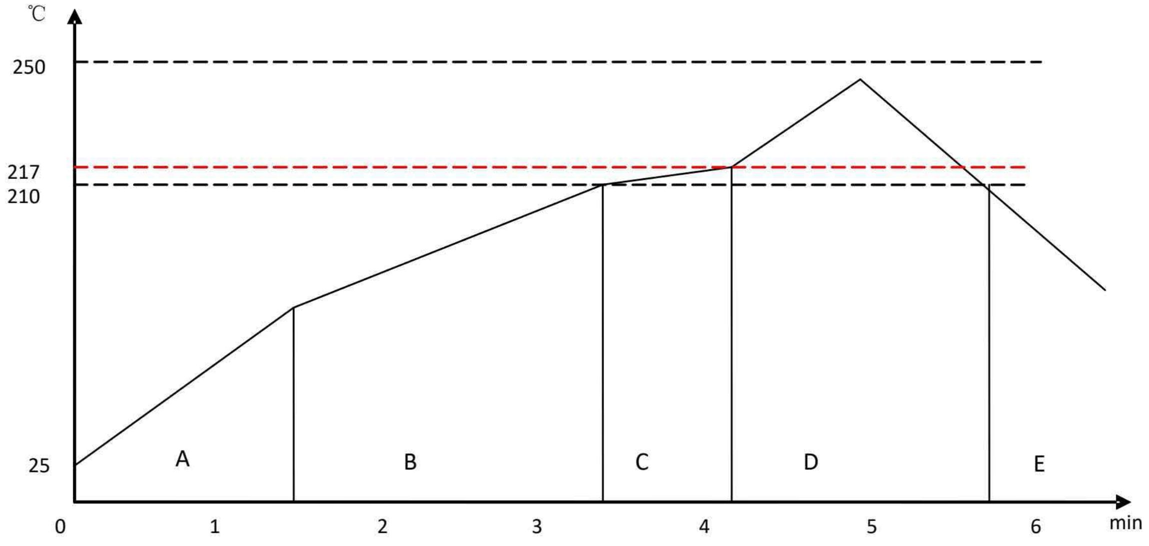


Figure 9: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 22mm(L) x 22mm(W) x 2.4mm(H) Tolerance: ±0.2mm
- Module size: 22mm x 22mm Tolerance: ±0.25mm
- Pad size: 1.8mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.2mm ±0.1mm
  (分板后边角残留板边误差：不大于0.5mm)

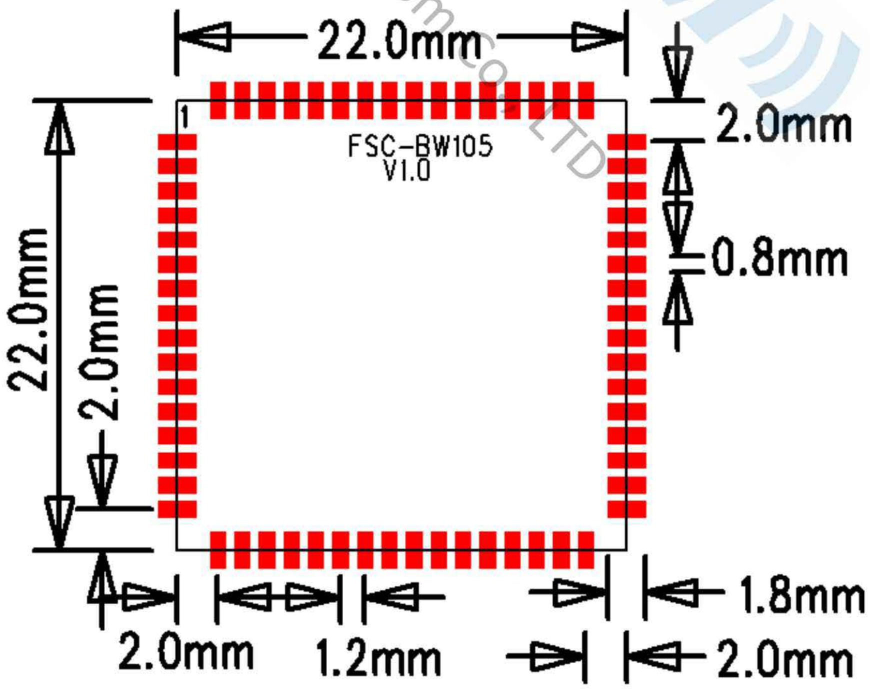


Figure 10: FSC-BW105 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, the ripple raised from 100/800mA step-response test should be small than 200mVpp.
  2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.
- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VBAT: 3.14 to 3.46V;   VDDIO: 1.71 to 3.46V

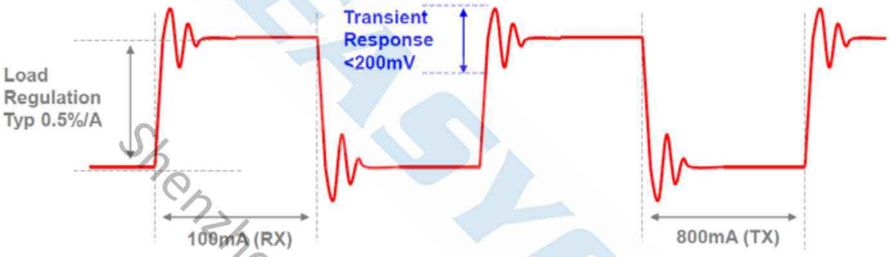


Figure 11: Requirement for the 3.3V power supply

9.2 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

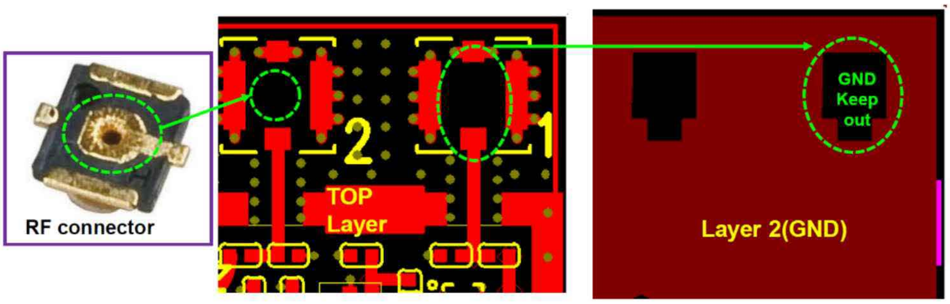


Figure 12: RF Circuit- RF pads

9.3 Soldering Recommendations

FSC-BW105 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.4 Layout Guidelines(Internal Antenna)

Important Note: The antenna of FSC-BW105 needs to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

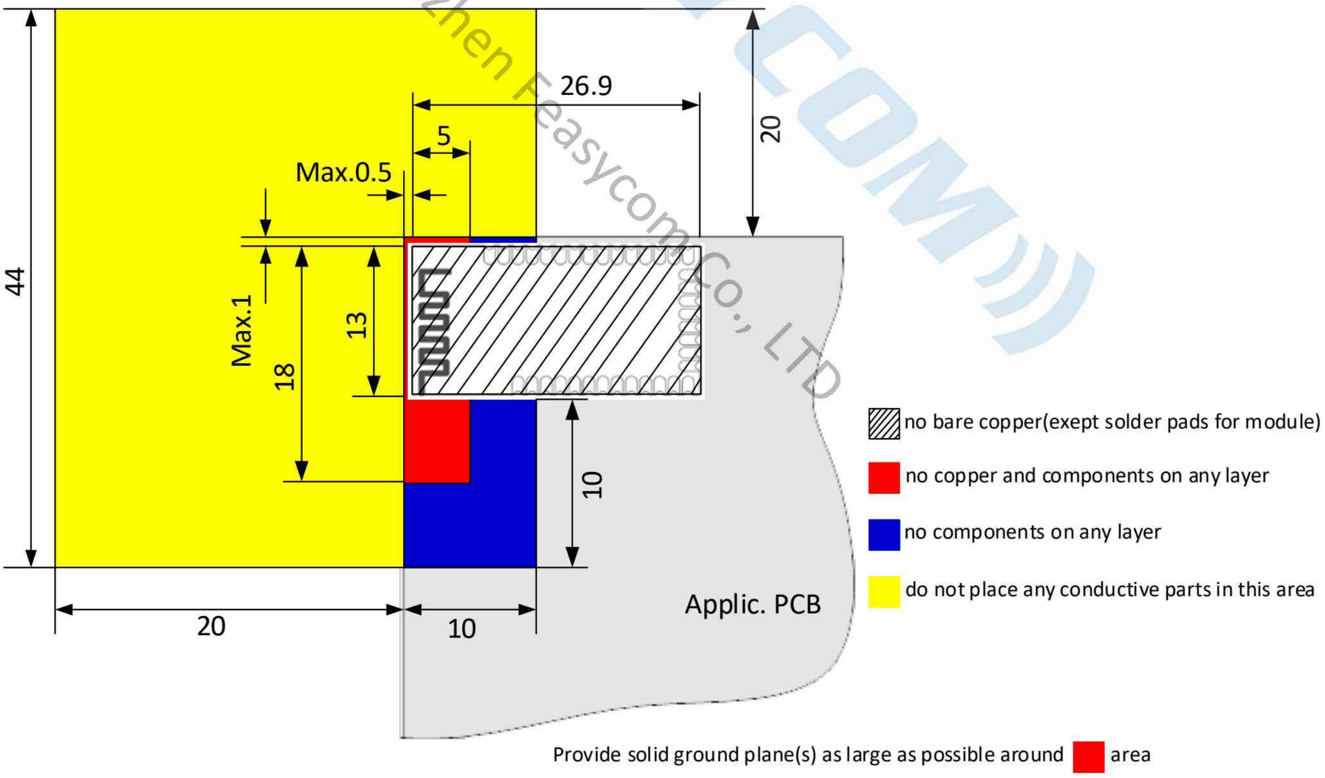


Figure 13: Restricted Area(Reference design) Unit: mm

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.5 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

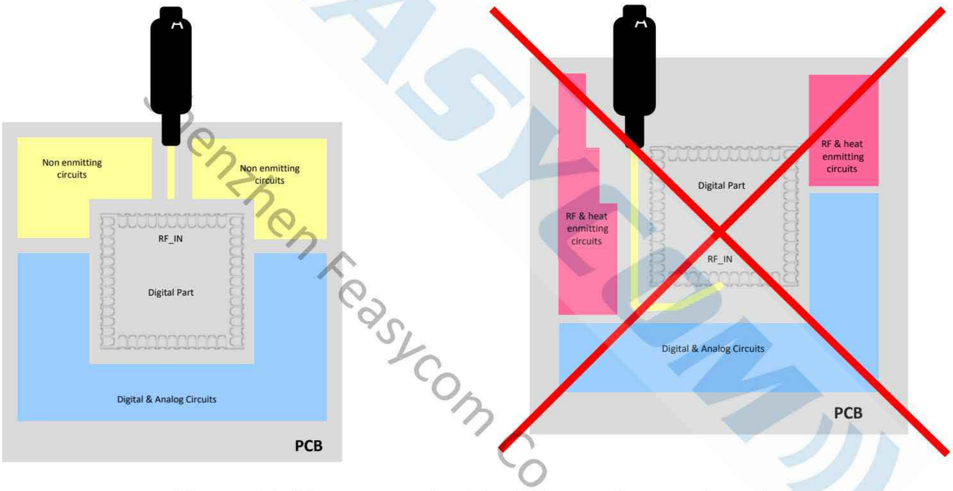


Figure 14: Placement the Module on a System Board

9.5.1 Antenna Connection and Grounding Plane Design

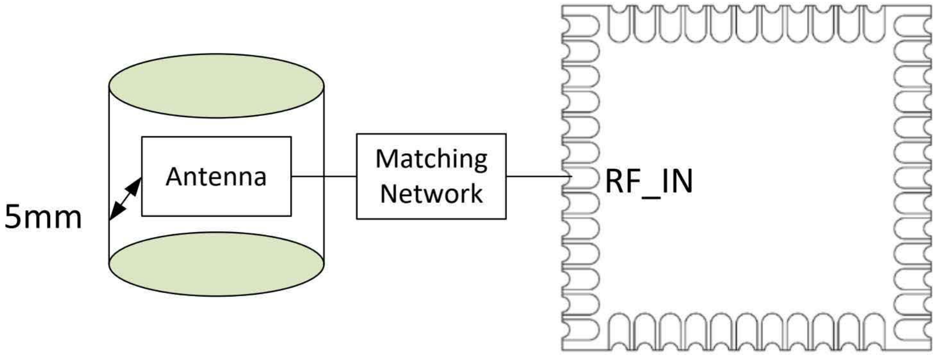


Figure 15: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

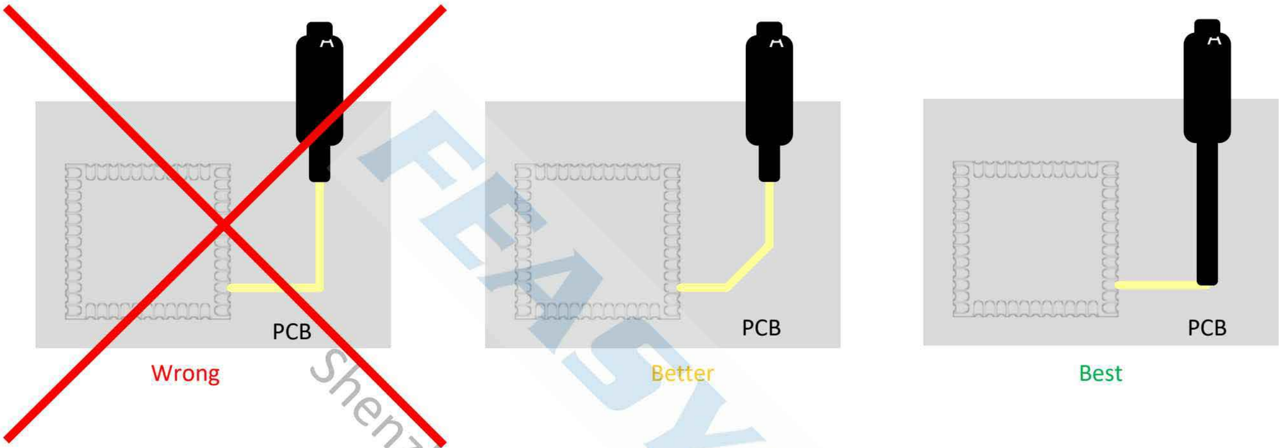


Figure 16: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.6 PCIe Lines Layout Guideline

PCIe_REFCLKP & PCIe_REFCLKN, PCIe_TXP & PCIe_TXN, PCIe_RXP & PCIe_RXN are the 3 differential pairs to be routed from host connector to FSC-BW105 with 100 Ohms differential Impedance.

Keep parallelism between PCIe_REFCLKP & PCIe_REFCLKN, PCIe_TXP & PCIe_TXN, and PCIe_RXP & PCIe_RXN with the trace spacing, common trace width / lengths to achieve 100 Ohms differential impedance.

Route the High Speed signals like Clock, PCIe_REFCLKP & PCIe_REFCLKN, PCIe_TXP & PCIe_TXN, PCIe_RXP &PCIe_RXN signals as equal and minimum possible trace lengths. Keep the maximum route spacing between PCIe signals and other signals.

Route the PCIe differential signals, on the Top side or Bottom side of the PCB, which is adjacent to the ground plane layer. Avoid plane splits under these high speed signals in the layout.

9.7 Power Trace Lines Layout Guideline

VBAT Trace Width: ⩾40mil

VDD_IO Trace Width: ⩾20mil

9.8 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW105 Module Ground Pads

Decoupling Capacitors close to FSC-BW105 Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

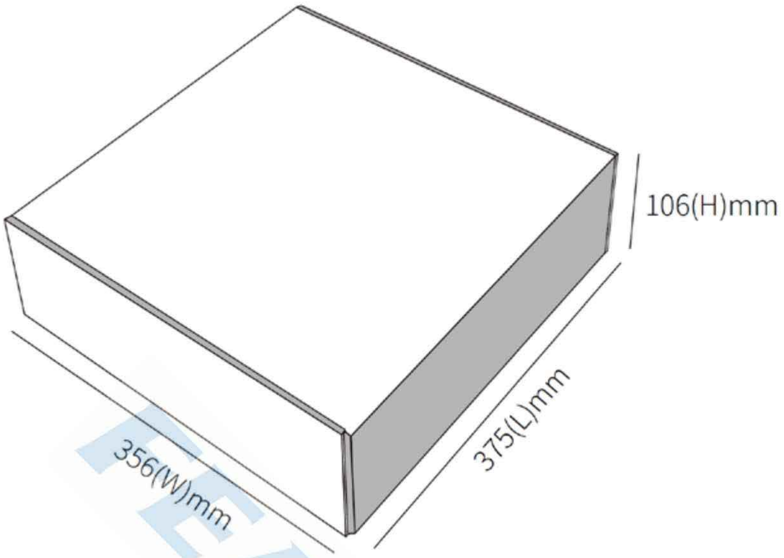
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 165mm * 315mm

Figure 17: Tray vacuum

10.2 Packing box(Optional)



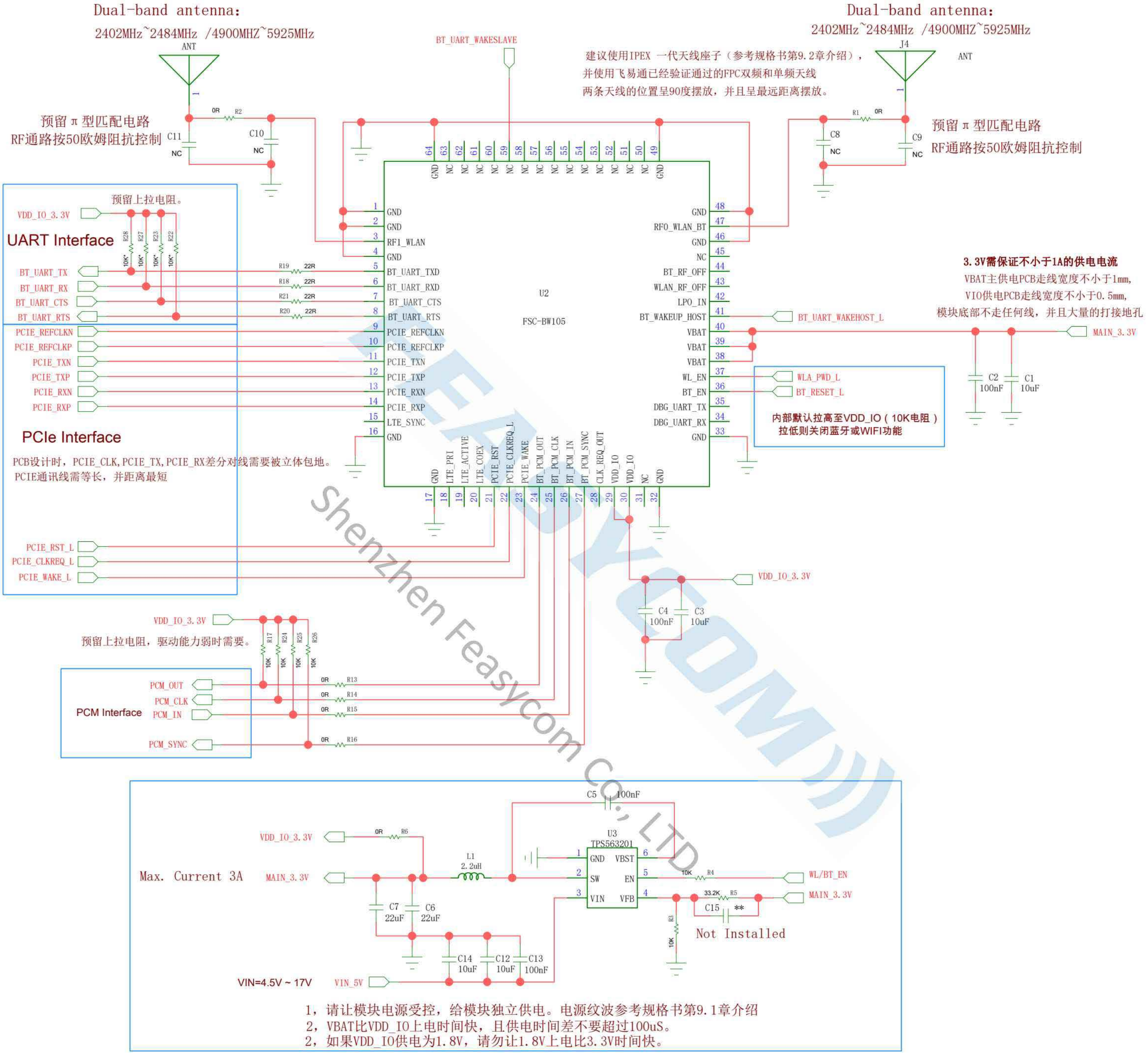
* If other packing is required, please confirm with the customer

* Packing: 500pcs per carton (Minimum packing quantity)

* **The outer packing size is for reference only, please refer to the actual size**

Figure 18: Packing Box

11. APPLICATION SCHEMATIC



预留π型匹配电路
RF通路按50欧姆阻抗控制

建议使用IPEX 一代天线座子（参考规格书第9.2章介绍），
并使用飞易通已经验证通过的FPC双频和单频天线
两条天线的位置呈90度摆放，并且呈最远距离摆放。

预留上拉电阻。

PCB设计时，PCIE_CLK,PCIE_TX,PCIE_RX差分对线需要被立体包地。
PCIE通讯线需等长，并距离最短

3.3V需保证不小于1A的供电电流
VBAT主供电PCB走线宽度不小于1mm,
VIO供电PCB走线宽度不小于0.5mm,
模块底部不走任何线，并且大量的打接地孔

内部默认拉高至VDD_IO（10K电阻）
拉低则关闭蓝牙或WIFI功能

预留上拉电阻，驱动能力弱时需要。

Not Installed

1，请让模块电源受控，给模块独立供电。电源纹波参考规格书第9.1章介绍
2，VBAT比VDD_IO上电时间快，且供电时间差不要超过100uS。
2，如果VDD_IO供电为1.8V，请勿让1.8V上电比3.3V时间快。