



FSC-BW246

2.4G WLAN 802.11 b/g/n
and Bluetooth 4.2 dual-mode Datasheet

Version 1.6

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Revision History

Version	Data	Notes	
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Contents

1. INTRODUCTION	5
2. GENERAL SPECIFICATION	6
3. HARDWARE SPECIFICATION	7
3.1 BLOCK DIAGRAM AND PIN DIAGRAM	7
3.2 PIN DEFINITION DESCRIPTIONS	8
4. PHYSICAL INTERFACE	9
4.1 GENERAL PURPOSE DIGITAL IO	9
4.2 RF INTERFACE	10
4.3 UART Interface	10
4.4 I2C Interface	11
4.5 ANALOG TO DIGITAL CONVERTER (ADC)	12
4.6 ETHERNET MAC INTERFACE	12
5. ELECTRICAL CHARACTERISTICS	12
5.1 ABSOLUTE MAXIMUM RATINGS	12
5.2 RECOMMENDED OPERATING CONDITIONS	13
5.3 RF POWER CONSUMPTION PARAMETERS	13
5.4 WI-FI RF	13
5.5 CLASSIC BLUETOOTH RF	14
5.5.1 Receiver-Basic Data Rate (BR)	14
5.5.2 Transmitter-Basic Data Rate (BR)	14
5.5.3 Receiver-Enhanced Data Rate (EDR)	15
5.5.4 Transmitter-Enhanced Data Rate (EDR)	15
5.6 BLUETOOTH LOW ENERGY RF	16
5.6.1 Receiver	16
5.6.2 Transmitter	16
6. MSL & ESD	17
7. RECOMMENDED TEMPERATURE REFLOW PROFILE	17
8. MECHANICAL DETAILS	18
8.1 MECHANICAL DETAILS	18
9. HARDWARE INTEGRATION SUGGESTIONS	19
9.1 SOLDERING RECOMMENDATIONS	19
9.2 LAYOUT GUIDELINES (INTERNAL ANTENNA)	19
9.3 LAYOUT GUIDELINES (EXTERNAL ANTENNA)	20
9.3.1 Antenna Connection and Grounding Plane Design	21
10. PRODUCT PACKAGING INFORMATION	22
10.1 DEFAULT PACKING	22
10.2 PACKING BOX (OPTIONAL)	23



11. DIFFERENCE FROM FSC-BW226	24
12. APPLICATION SCHEMATIC.....	24

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1. INTRODUCTION

Overview

FSC-BW246 is a highly integrated single-chip 2.4GHz wireless LAN (WLAN) and Bluetooth low energy (v4.2) communication controller. It uses a 32-bit MCU single/dual-core processor with a computing power of up to 600 MIPS, a WLAN baseband with 1T1R function, RF, Bluetooth and peripheral devices.

FSC-BW246 is an appropriate product for designers who want to add wireless capability to their products.

Support for external antennas and increase wireless coverage.

Wi-Fi Features

- 802.11 b/g/n
- 802.11 n (2.4GHz) speed up to 150 Mbps
- Wireless Multimedia (WMM)
- Frame aggregation (TX/RX A-MPDU, RX A-MSDU)
- Immediate Block ACK
- Reorganization (Defragmentation)
- Beacon automatic monitoring (hardware TSF)
- Antenna diversity

Bluetooth features

- Bluetooth V4.2
- Up to +9 dBm output power
- NZIF receiver has BLE reception sensitivity of -94 dBm
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART interface
- CVSD and SBC audio codec algorithms
- Bluetooth Piconnet and Scatternet
- Multi-device connection supporting traditional Bluetooth and Bluetooth low energy

- Support simultaneous broadcast and scan
- Support SPI/I2S/I2C/UART/PWM/Ethernet MAC/ADC interface
- Stamp hole package
- Low power consumption
- Support standard level 1, level 2 and level 3
- The default UART baud rate is 921.6Kbps, which can support 9600bps to 500Kbps
- Support air upgrade
- Bluetooth profile support: SPP, HID, GATT, ATT, GAP
- Support iBeacon
- Support external antenna stamp port or ipex connection
- RoHS Compliant

Application

- Home automation
- Automated industry
- Audio equipment
- Wi-Fi toys
- Wearable electronics
- POS system

Module picture as below showing



Figure 1: FSC-BW246 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth	Version : V4.2
		Frequency : 2.412 - 2.484 GHz
		Transmit Power: +9 dBm (Maximum)
	WiFi	802.11 b/g/n 1x1, 2.4GHz
		Frequency : 2.412 ~ 2.484GHz
		Transmit Power(2.4GHZ): +20.5 dBm(11 b), 18 dBm(11 n) MCS0-7 supports 20MHz and 40MHz bandwidth
Host Interface and Peripherals	UART Interface	Adjustable transmit power
		TX, RX (Auto Flow Control)
		General Purpose I/O
		Default 921600,N,8,1
	GPIO	Baudrate support from 9600 to 5000000bps
		7, 8 data bit character
		18 (maximum – configurable) lines
		O/P drive strength (4 mA)
	I2C Interface	Pull-up resistor (45 KΩ) control
		Read pin-level
	SPI Interface	1 (configurable from GPIO total).
		Standard mode (100Kbit/s); High-speed mode (400Kbit/s)
Profiles	Classic Bluetooth	Support Master/Slave mode
		16-bit resolution
	Bluetooth Low Energy	Accurately capture external timed events
		Supports PWM interrupts
Maximum Connections	Classic Bluetooth	Support
	Bluetooth Low Energy	Support
FW upgrade	WiFi	WiFi-AP(access point), WiFi-Station
	Classic Bluetooth	TBD
Supply Voltage	Bluetooth Low Energy	TBD
	Supply	UART
Power Consumption	Bluetooth	2.3 ~ 3.6V
		Send BT/BLE, POUT = 0dBm, power consumption is 130mA
	WiFi	Receive BT/BLE, power consumption is 95 ~ 100mA
		Send 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm, power consumption is 240mA
		Send 802.11g, OFDM 54 Mbps, POUT = +16 dBm, power consumption is 190mA
		Send 802.11n, OFDM MCS7, POUT = +14 dBm, power consumption is 180mA
Physical	Dimensions	Receive 802.11b/g/n, power consumption is 95 ~ 100mA
		13mm X 26.9mm X 2.2mm; Pad Pitch 1.5mm

Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model:	Class-2
	Machine Model:	Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

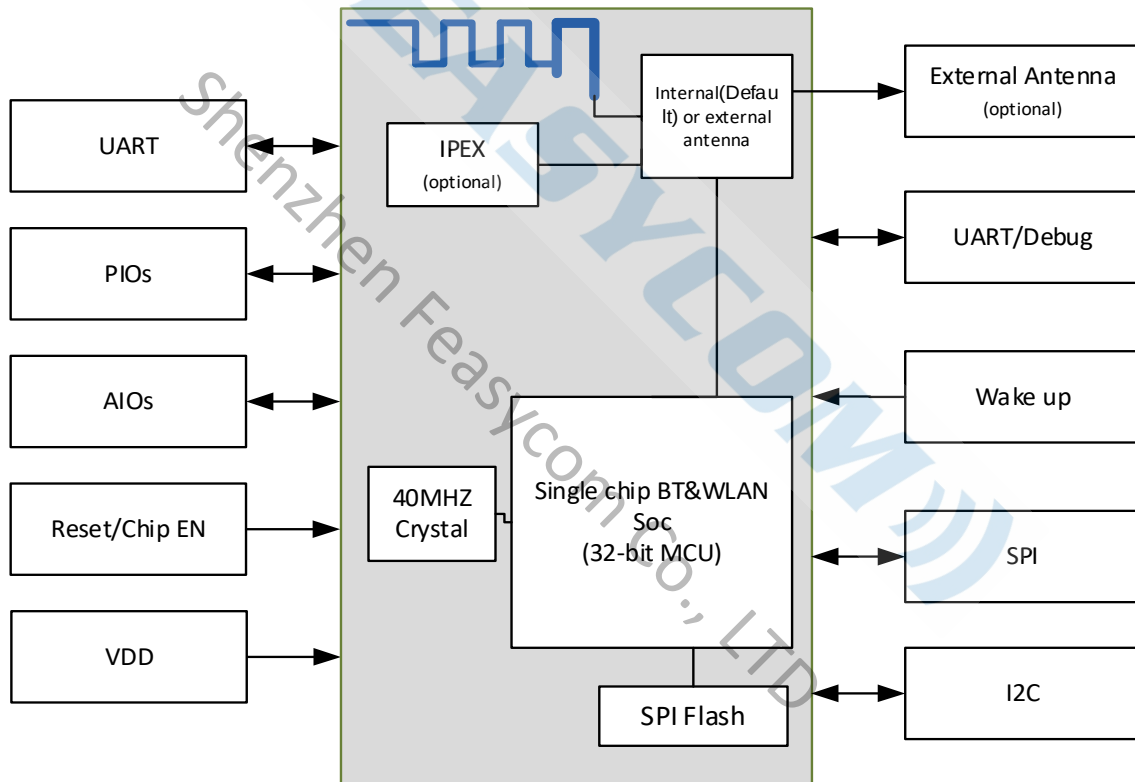


Figure 2: Block Diagram

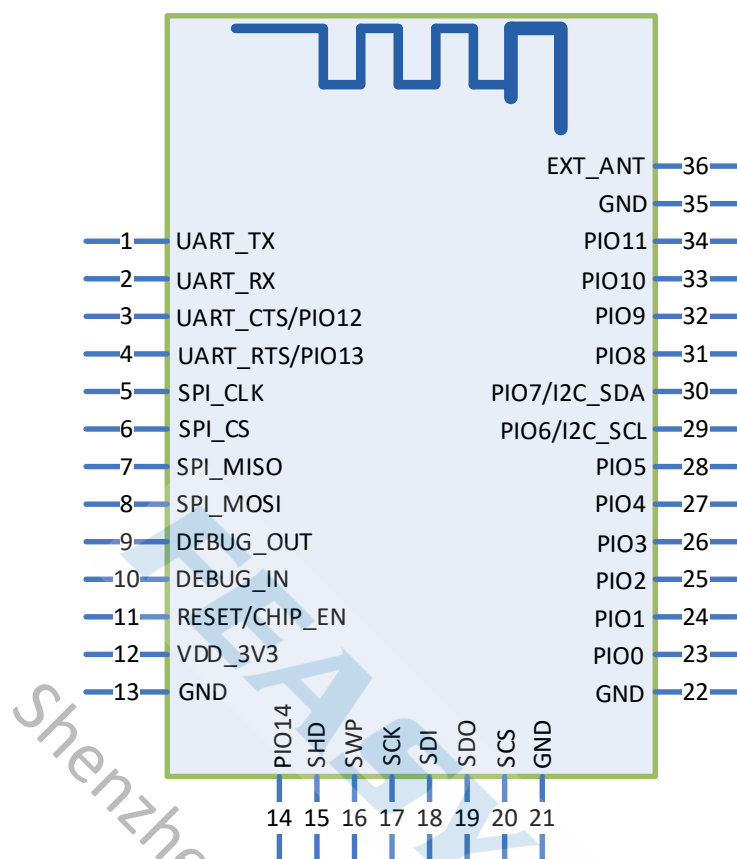


Figure 3: FSC-BW246 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions
1	UART_TX	O	UART Data output
2	UART_RX	I	UART Data input
3	UART_CTS/PIO12	I/O	Programmable input/output line Alternative Function 1: UART Clear to Send (active low)
4	UART_RTS/PIO13	I/O	Programmable input/output line Alternative Function 1: UART Request to Send (active low)
5	SPI_CLK	I/O	SPI_CLK Alternative Function 1: Programmable input/output line
6	SPI_CS	I/O	SPI_MOSI Alternative Function 1: Programmable input/output line
7	SPI_MISO	I/O	SPI_MISO Alternative Function 1: Programmable input/output line
8	SPI_MOSI	I/O	SPI_CS Alternative Function 1: Programmable input/output line
9	DEBUG_OUT	I/O	Debug Interface (Data OUT)
10	DEBUG_IN	I/O	Debug Interface (Data IN)
11	RESET/CHIP_EN	I	External reset input: Active LOW, Set this pin low reset the module.

12	VDD_3V3	VDD	Power supply voltage 2.3 ~ 3.3V
13	GND	VSS	Power Ground
14	PIO14	I	Input pin
15	SHD	I/O	SPI_HOLD interface inside the module
16	SWP	I/O	SPI_WP interface inside the module
17	SCK	I/O	SPI_SCLK interface inside the module
18	SDI	I/O	SPI_SI interface inside the module
19	SDO	I/O	SPI_SO interface inside the module
20	SCS	I/O	SPI_CS interface inside the module
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	PIO0	I/O	Programmable input/output line Default pull down
24	PIO1	I/O	Programmable input/output line Default pull up
25	PIO2	I/O	Programmable input/output line Default pull down
26	PIO3	I/O	Programmable input/output line Default pull up
27	PIO4	I/O	Programmable input/output line Default pull up
28	PIO5	I/O	Programmable input/output line
29	PIO6/I2C_SCL	I/O	Programmable input/output line Alternative Function: I2C_SCL(Default)
30	PIO7/I2C_SDA	I/O	Programmable input/output line Alternative Function: I2C_SDA(Default)
31	PIO8	I/O	Programmable input/output line
32	PIO9	I/O	Programmable input/output line Bluetooth LED (minimum) is not connected and blinking, the connection is always on
33	PIO10	I/O	Programmable input/output line Wi-Fi LED (default) flashes when not connected, the connection is always on
34	PIO11	I/O	Programmable input/output line
35	GND	VSS	RF Ground
36	EXT_ANT	O	RF signal output

4. PHYSICAL INTERFACE

4.1 General Purpose Digital IO

The module has a total of 18 GPIO pins. By configuring the corresponding registers, these pins can be assigned different functions, including the following types of GPIO:

Only GPIO with digital function, GPIO with analog function, GPIO with capacitive touch function, etc. GPIO with analog function and GPIO with capacitive touch function can be configured as digital GPIO.

Most GPIOs with digital functions can be configured as internal pull-up/pull-down or set to high impedance. When configured as an input, the input value can be obtained by reading the register. Input pins can also be set to generate CPU interrupts by edge triggering or level triggering.

4.2 RF Interface

For This Module, the default mode for antenna is internal , it also has the interface for external antenna, or use an IPEX interface to connect an external antenna. If you need to use an external antenna, by modifying the module on the OR resistance to block out the on-board antenna. Or indicate your request when placing an order.

The user can connect a 50 ohm antenna directly to the RF port.

Bluetooth basic parameter:

- Level 1, 2 and 3 transmit power, dynamic control range up to 24 dB
- π 4 DQPSK and 8 DPSK modulation
- NZIF receiver has high sensitivity and dynamic range exceeding 94 dBm
- Supports Class-1 operation without external PA
- ACL, SCO, eSCO and AFH
- Transmit power -12dBm ~ +9dBm

WiFi basic parameter:

- 802.11b/g/n
- 802.11n MCS0-7 supports 20 MHz and 40 MHz bandwidth
- Data rate up to 150 Mbps
- Receive STBC 2×1
- Transmit power up to 20.5 dBm
- Adjustable transmit power
- 802.11b wireless transmission power up to +20.5 dBm
- 802.11n wireless transmission power up to +18 dBm

4.3 UART Interface

The four signal pins are used to implement the UART function. When FSC-BW246 is connected to another digital device, UART_RX and UART_TX transmit data between the two devices. The remaining two pins UART_CTS and UART_RTS can be used to implement RS232 hardware flow control, and both are low-level effective, that is, transmission is allowed when the level is low, and transmission is stopped when the level is high.

Table 3: Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 9600bps ($\leq 2\%$ Error)
	Standard 921600bps($\leq 1\%$ Error)
	Maximum 5000000bps($\leq 1\%$ Error)
Flow control	RTS/CTS
Parity	None, Odd or Even

Number of stop bits	1 / 2
Bits per channel	7/8

When connecting the module to a host, please make sure to follow .

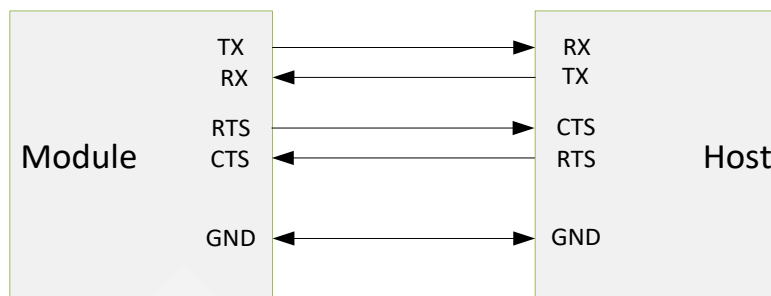


Figure 4: UART Connection

4.4 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

- Up to two I2C bus interfaces, supporting master mode and slave mode, the frequency can be up to 400KHZ.
- 7-bit/10-bit addressing mode
- Dual addressing mode

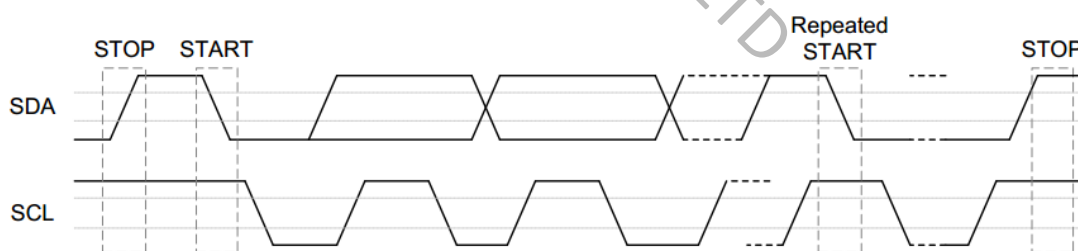


Figure 5: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.5 Analog to Digital Converter (ADC)

The device integrates a 12-bit 1us multichannel ADC. The conversion range is $0V < V_{DDA} < 3.6V$. The analog watchdog module can be used to detect channels that need to be kept within a specific threshold window. The configurable channel management module for analog inputs can also be used to perform conversions in single, continuous, scan, or discontinuous mode to support more advanced usage. The ADC can be triggered by events generated by an internally connected general-purpose timer (TMx) and advanced control timer (TM1). Temperature sensors can be used to generate voltages that vary linearly with temperature. Each device is factory calibrated to improve accuracy, and calibration data is stored in the system storage area.

- 12-bit SAR ADC engine, conversion rate up to 1 MSPS
- Conversion range: VSSA to VDDA (2.6 to 3.6V)
- Temperature Sensor

4.6 Ethernet MAC interface

FSC-BW246 provides a media access controller (MAC) interface that complies with the IEEE-802.3-2008 standard for Ethernet communications. FSC-BW246 requires an external physical layer interface chip (PHY) to connect the physical LAN bus (twisted pair, optical fiber, etc.). The physical layer interface chip is connected to the chip through 17 MII signals or 9 RMII signals. The Ethernet MAC interface (EMAC) supports the following features:

- To 10 Mbps and 100 Mbps
- Dedicated DMA controller realizes high-speed transmission between Ethernet MAC interface and dedicated SRAM
- Tagged MAC frame (support VLAN)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frame)
- 32-bit CRC automatic generation and elimination
- Multiple address filtering modes for unicast and multicast addresses (broadcast and group addresses)
- Record the 32-bit status code of each frame sent and received
- The internal FIFO is used to buffer transmitted and received frames.
- Both transmit FIFO and receive FIFO are 512 words (32-bit)
- Hardware PTP (Precision Time Protocol) compliant with IEEE 1588 2008 (PTP V2) standard
- 25 MHz/50 MHz clock output

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V _{IN} - I/O supply voltage (VDDIO)	-0.3	+3.6	V
V _{IN} - VIN-Analog/Digital Supply Voltage (VDD)	-0.3	+3.6	V
T _{OT} - Operating temperature	-40	+85	°C
T _{ST} - Storage temperature	-40	+85	°C

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V _{IN} - Core supply voltage (VDD)	2.3	3.3	3.6	V
I _{IN} - Supply current of external power supply	0.5	-	-	A

5.3 RF power consumption parameters

The following power consumption data is based on the test results completed at the RF interface with a 3.3 V power supply and an ambient temperature of 25 °C. All launch data is based on 50% the duty cycle is measured.

Table 6: RF power consumption parameters

Mode	Min	Type	Max	Unit
Send 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm	-	240	-	mA
Send 802.11g, OFDM 54 Mbps, POUT = +16 dBm	-	190	-	mA
Send 802.11n, OFDM MCS7, POUT = +14 dBm	-	180	-	mA
Receive 802.11b/g/n	-	95 ~ 100	-	mA
Send BT/BLE, POUT = 0 dBm	-	130	-	mA
Receive BT/BLE	-	95 ~ 100	-	mA

5.4 Wi-Fi RF

Table 7: Wi-Fi radio frequency characteristics

Parameter	Mode	Min	Type	Max	Unit
Working frequency	-	2412	-	2484	MHz
Output impedance	-	-	30+j10 Ω	-	Ω
Output Power	11n, MCS7	12	13	14	dBm
	11b Mode	18.5	19.5	20.5	dBm
Sensitivity	11b, 1 Mbps	-	-98	-	dBm
	11b, 11 Mbps	-	-88	-	dBm
	11g, 6 Mbps	-	-93	-	dBm
	11g, 54 Mbps	-	-75	-	dBm
	11n, HT20, MCS0	-	-93	-	dBm
	11n, HT20, MCS7	-	-73	-	dBm

Adjacent channel suppression	11n, HT40, MCS0	-	-90	-	dBm
	11n, HT40, MCS7	-	-70	-	dBm
	11g, 6 Mbps	-	27	-	dB
	11g, 54 Mbps	-	13	-	dB
	11n, HT20, MCS0	-	27	-	dB
	11n, HT20, MCS7	-	12	-	dB

5.5 Classic Bluetooth RF

5.5.1 Receiver-Basic Data Rate (BR)

Table 8: Receiver characteristics – basic data rate (BR)

Parameter	Condition	Min	Type	Max	Unit
Sensitivity@0.1% BER	-	-90	-89	-88	dBm
Maximum received signal@0.1% BER	-	0	-	-	dBm
Co-channel rejection ratio C/I	-	-	+7	-	dB
Adjacent channel selective suppression ratio C/I	$F = F_0 + 1 \text{ MHz}$	-	-	-6	dB
	$F = F_0 - 1 \text{ MHz}$	-	-	-6	dB
	$F = F_0 + 2 \text{ MHz}$	-	-	-25	dB
	$F = F_0 - 2 \text{ MHz}$	-	-	-33	dB
	$F = F_0 + 3 \text{ MHz}$	-	-	-25	dB
	$F = F_0 - 3 \text{ MHz}$	-	-	-45	dB
Out-of-band blocking	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	36	-	-	dBm

5.5.2 Transmitter-Basic Data Rate (BR)

Table 9: Transmitter characteristics – basic data rate (BR)

Parameter	Condition	Min	Type	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	-12	-	+9	dBm
20 dB bandwidth	-	-	0.9	-	MHz
Adjacent channel transmit power	$F = F_0 \pm 2 \text{ MHz}$	-	-47	-	dBm
	$F = F_0 \pm 3 \text{ MHz}$	-	-55	-	dBm
	$F = F_0 \pm > 3 \text{ MHz}$	-	-60	-	dBm
Δf_{1avg}	-	-	-	-155	kHz
Δf_{2max}	-	133.7	-	-	kHz
$\Delta f_{2avg}/\Delta f_{1avg}$	-	-	0.92	-	-
ICFT	-	-	-7	-	kHz

Drift rate	-	0.7	-	kHz/50_s
Offset (DH1)	-	6	-	kHz
Offset (DH5)	-	6	-	kHz

5.5.3 Receiver-Enhanced Data Rate (EDR)

Table 10: Receiver characteristics-enhanced data rate (EDR)

Parameter	Condition	Min	Type	Max	Unit
π 4 DQPSK					
Sensitivity@0.01% BER	-	-90	-9+	-99	dBm
Maximum received signal @0.01% BER	-	-	0	-	dBm
Co-channel rejection ratio C/I	-	-	11	-	dB
Adjacent channel selective suppression ratio C/I	F = F0 + 1 MHz	-	-7	-	dB
	F = F0 - 1 MHz	-	-7	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
8DPSK					
Sensitivity@0.01% BER	-	-84	-83	-82	dBm
Maximum received signal @0.01% BER	-	-	-5	-	dBm
Co-channel rejection ratio C/I	-	-	18	-	dB
Adjacent channel selective suppression ratio C/I	F = F0 + 1 MHz	-	2	-	dB
	F = F0 - 1 MHz	-	2	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-25	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-38	-	dB

5.5.4 Transmitter-Enhanced Data Rate (EDR)

Table 11: Transmitter characteristics-enhanced data rate (EDR)

Parameter	Condition	Min	Type	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dB
π 4 DQPSK max w0	-	-	-0.72	-	kHz
π 4 DQPSK max wi	-	-	-6	-	kHz
π 4 DQPSK max wi + w0	-	-	-7.42	-	kHz
8DPSK max w0	-	-	0.7	-	kHz
8DPSK max wi	-	-	-9.6	-	kHz
8DPSK max wi + w0	-	-	-10	-	kHz

π 4 DQPSK modulation accuracy	RMS DEVM	-	4.28	-	%
	99% DEVM	-	100	-	%
	Peak DEVM	-	13.3	-	%
8 DPSK modulation accuracy	RMS DEVM	-	5.8	-	%
	99% DEVM	-	100	-	%
	Peak DEVM	-	14	-	%
In-band spurious emissions	$F = F_0 \pm 1 \text{ MHz}$	-	-46	-	dBm
	$F = F_0 \pm 2 \text{ MHz}$	-	-40	-	dBm
	$F = F_0 \pm 3 \text{ MHz}$	-	-46	-	dBm
	$F = F_0 + / - > 3 \text{ MHz}$	-	-	-53	dBm
EDR differential phase encoding		-	-100	-	%

5.6 Bluetooth Low Energy RF

5.6.1 Receiver

Table 12: Low-power Bluetooth receiver features

Parameter	Condition	Min	Type	Max	Unit
Sensitivity@30.8% PER	-	-94	-93	-92	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel rejection ratio C/I	-	-	+10	-	dB
Adjacent channel suppression ratio C/I	$F = F_0 + 1 \text{ MHz}$	-	-5	-	dB
	$F = F_0 - 1 \text{ MHz}$	-	-5	-	dB
	$F = F_0 + 2 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 2 \text{ MHz}$	-	-35	-	dB
	$F = F_0 + 3 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 3 \text{ MHz}$	-	-45	-	dB
Out-of-band blocking	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.6.2 Transmitter

Table 13: Low-power Bluetooth transmitter features

参数	条件	最小值	典型	最大值	单位
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	-10	-	+9	dBm
Adjacent channel transmit power	$F = F_0 \pm 2 \text{ MHz}$	-	-52	-	dBm
	$F = F_0 \pm 3 \text{ MHz}$	-	-58	-	dBm
	$F = F_0 \pm > 3 \text{ MHz}$	-	-60	-	dBm
Δf_{1avg}	-	-	-	265	kHz

Δf_{2max}	-	247	-	-	kHz
$\Delta f_{2avg}/\Delta f_{1avg}$	-	-	0.92	-	
ICFT	-	-	-10	-	kHz
Drift speed	-	-	0.7	-	kHz/50_s
Offset	-	-	2	-	kHz

6. MSL & ESD

Table 14: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccant (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccant and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 15: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit
	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

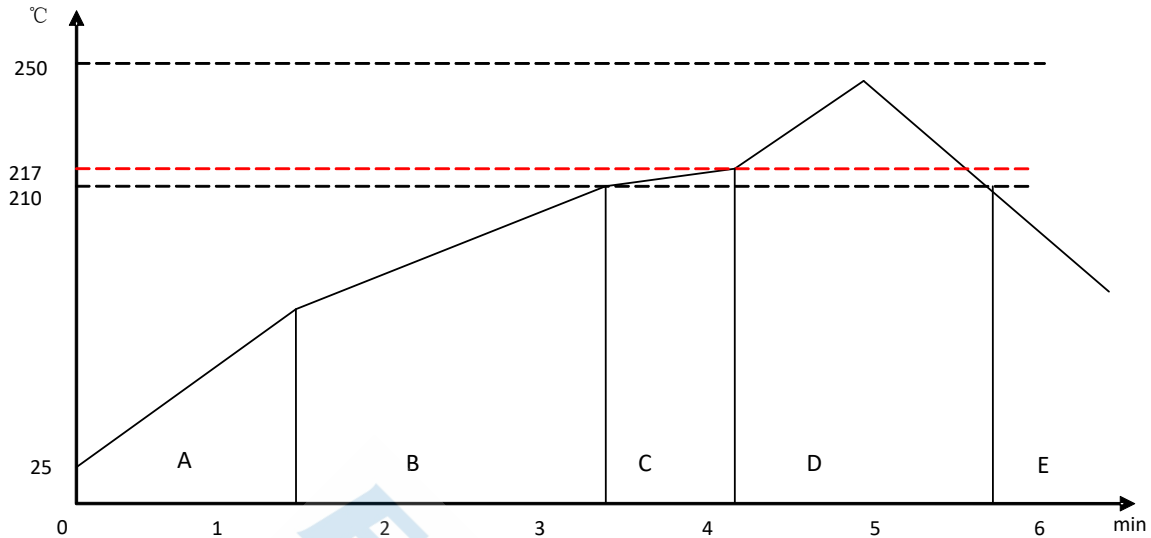


Figure 6: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (T_p) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: $\pm 0.1\text{mm}$
- Module size: 13mm X 26.9mm Tolerance: $\pm 0.2\text{mm}$
- Pad size: 1mmX0.8mm Tolerance: $\pm 0.2\text{mm}$
- Pad pitch: 1.5mm Tolerance: $\pm 0.1\text{mm}$

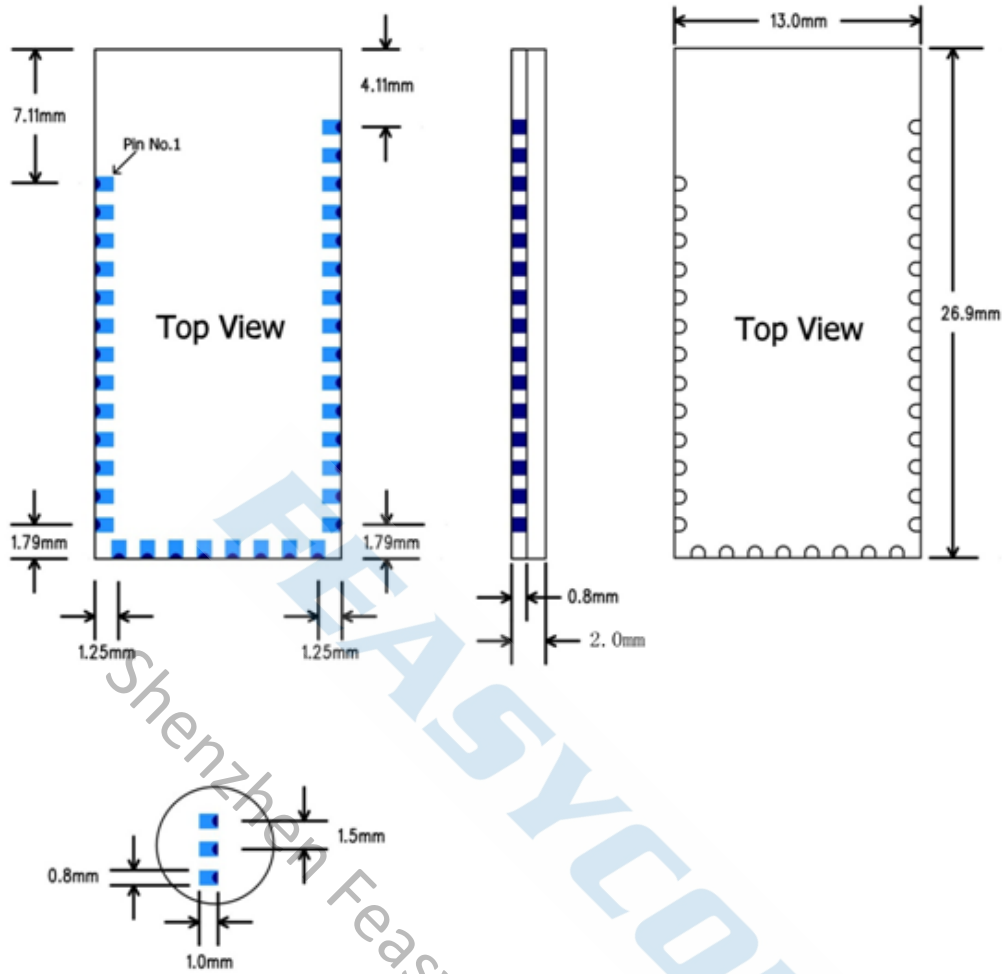


Figure 7: FSC-BW246 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW246 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

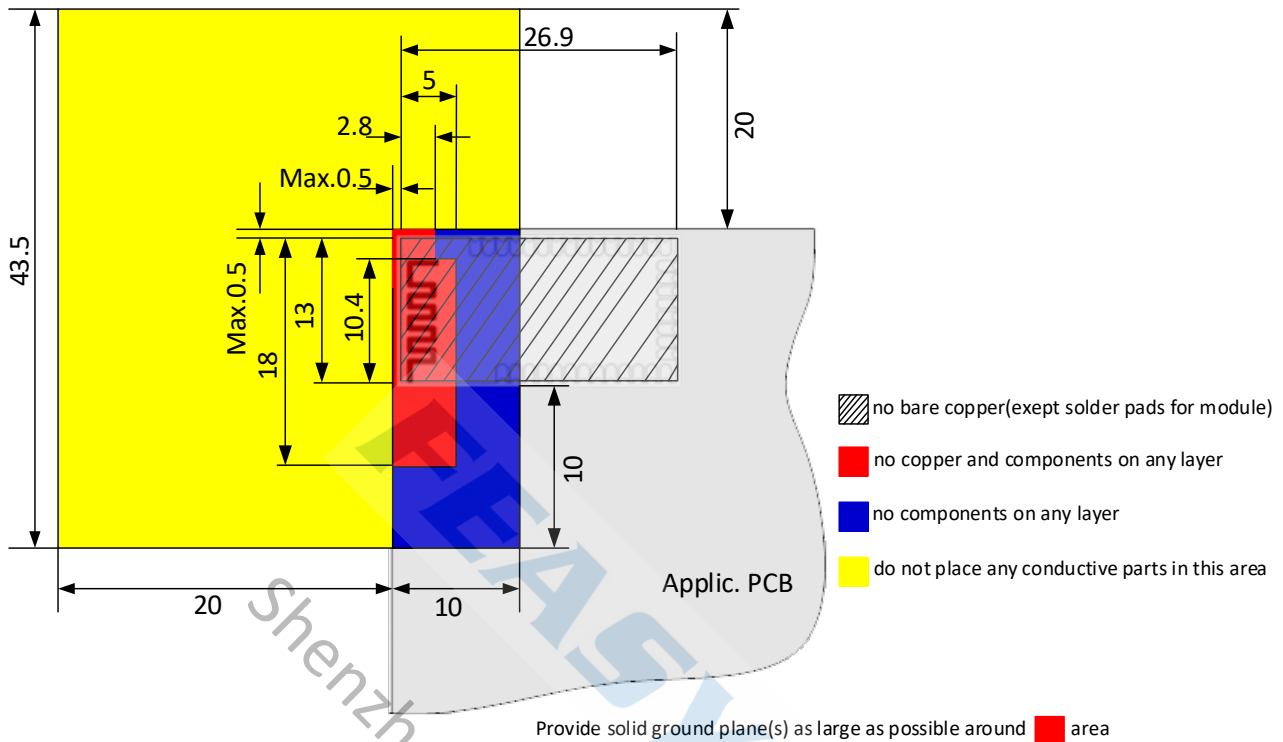


Figure 8: FSC-BW246 Restricted Area (Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

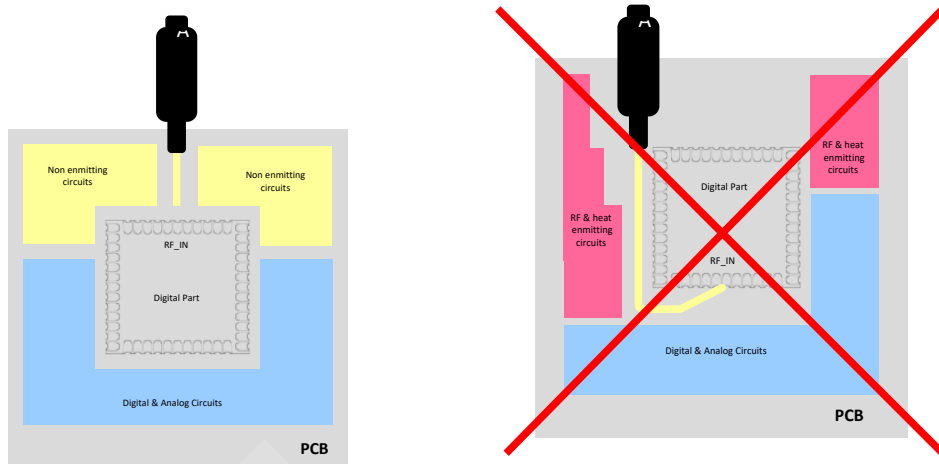


Figure 9: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

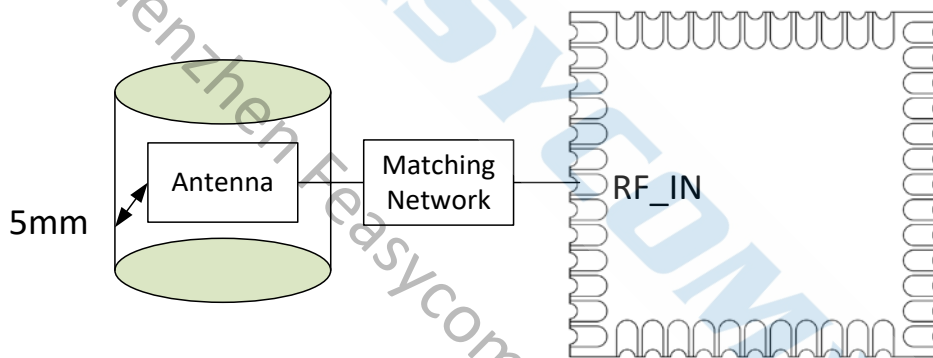


Figure 10: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

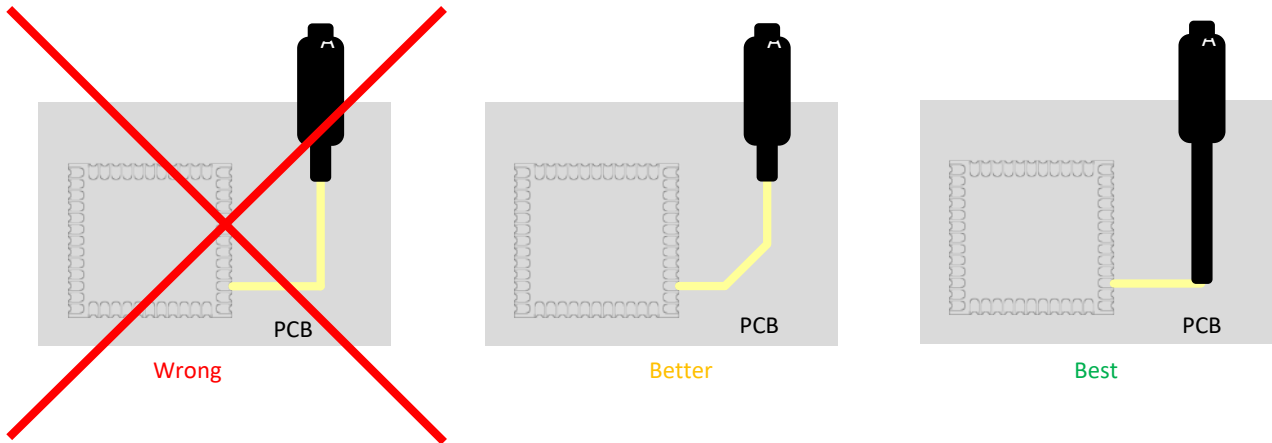


Figure 11: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

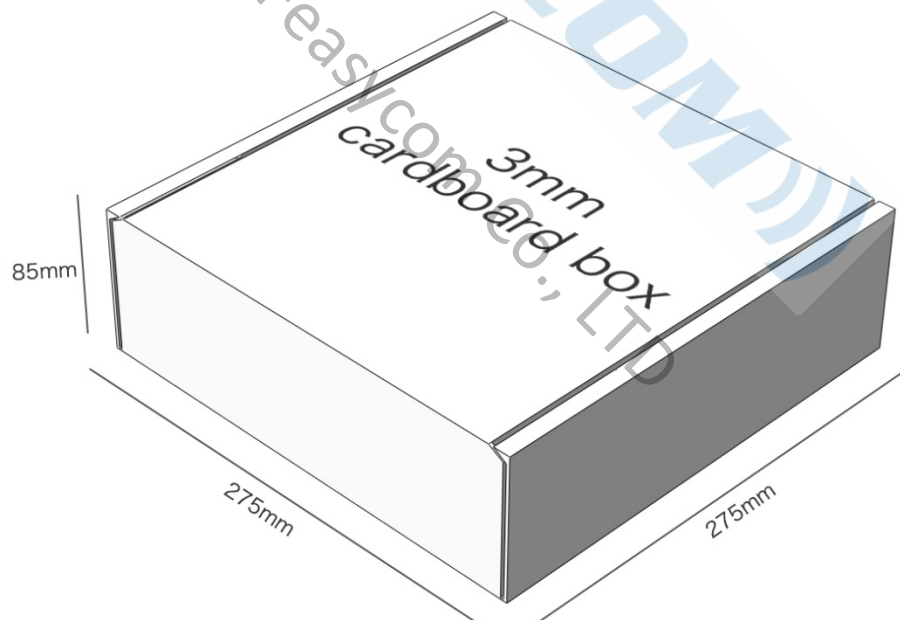
- Tray vacuum
- Tray Dimension: 180mm * 195mm





Figure 12: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 13: Packing Box

11. Difference from FSC-BW226

The 18 and 20 pins of FSC-BW226 are grounded by default, while the 18 and 20 pins of FSC-BW246 are internal flash pins. If connected to the ground, BW246 will not work normally. Please pay attention!

12. APPLICATION SCHEMATIC

