FSC-BW256B

Wi-Fi 6 + BT 5.4 Dual Mode SoC Module Datasheet

Version 1.5

Revision History

Version	Data	Notes	
1.0	2024/03/21	Initial Version	Mo
1.1	2024/06/07	Update the application schematic	Mo
1.2	2024/07/19	Update module picture, flash parameters and baud rate	Li
1.3	2024/08/30	Update the general specifications and layout guidelines	Li
1.4	2024/09/21	Update module picture	Li
1.5	2025/03/10	Update module picture（with shielding cover）	Li

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Contents

1. INTRODUCTION

Overview

The FSC-BW256B module adopts a high-performance SOC, which is an industry's leading WIFI6 / BT5.4 dual-mode single chip. It supports all WIFI6 standards while boasting the lowest power consumption in the industry.Additionally, the FSCBW256B integrates a Cort exM4F CPU with a main frequency that can reach 480 MHz.With the help of the internal integrated 992KB SRAM, 896KB ROM and up to 32Mbits on-chip SPI flash memory, the module provides users with powerful hardware support and enables secondary development. The module also provides a variety of peripheral interfaces—SPI, SDIO, I2C, and UART—for control and data transmission, making it versatile and easily adaptable to any microcontroller-based design.

The FSC-BW256B module supports the IEEE802.11 b/g/n/a/ac/ax protocol and the complete TCP/IP protocol stack. Users can leverage this module to integrate networking capabilities into existing equipment or develop standalone network controllers.

By providing maximum practicality at a competitive cost, the FSCBW256B module opens up limitless possibilities for integrating Wi-Fi functionality into diverse systems.

Wi-Fi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Wi-Fi 6 support 2.4GHz/5GHz Frequency band
- The highest data rate is 286.8Mbps with 20/40MHz bandwidth
- Support 5MHz/10MHz mode
- RX sensitivity under 11b 1M mode -97dBm
- Tx power up to 20dBm in 11b mode, up to 18dBm in HT/VHT/HE MCS7 mode
- Support STA, AP, Wi-Fi Direct mode at the same time
- Support STBC, beamforming
- Support Wi-Fi6 TWT
- Support two NAVs, buffer report, space reuse, Multi-BSSID, power saving in PPDU
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, medium code, UORA
- Support WEP / WPA / WPA2 / WPA3-SAE Personal, MFP Frequency band

BT 5.4 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/3.0/4.x/5.3/5.4
- Supports advanced master and slave topologies

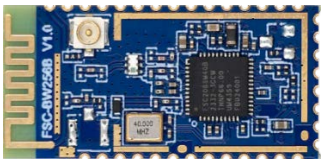
CPU Features

- Integrated Cortex-M4F CPU with MPU and FPU
- On-chip memory includes 992KB SRAM and 896KB ROM
- Supports SDIO3.0/SPI/USB2.0
- Integrated hardware crypto accelerator AES /HASH
- Integrated True Random Number Generator (TRNG)
- Integrated 32mbits SPI flash
- Integrated UART/I2S/I2C/PWM/SPI/SDMMC
- Integrated watchdog
- Support free RTOS

Applications

- IoT devices
- Wireless devices

Module picture as below showing

Order Number	Descriptions	Module picture as below showing
FSC-BW256B (Default)	Bluetooth (onboard built-in antenna) Wi-Fi (IPEX connector external antenna) Dimension: 13mm × 26.9 mm ×2.0mm (without shielding cover)	
FSC-BW256B_1 (Optional)	Bluetooth (onboard built-in antenna) Wi-Fi (IPEX connector external antenna) Dimension: 13mm × 26.9 mm ×2.3mm (with shielding cover)	
FSC-BW256B_2 (Optional)	Bluetooth (IPEX connector external antenna) Wi-Fi (IPEX connector external antenna) Dimension: 13mm × 26.9 mm ×2.3mm (with shielding cover)	

2. General Specifications

Table 2-1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.4 LE & BR/EDR
Frequency Band		2402MHz~2480MHz
Interface		UART
WIFI		
WiFi Standard		802.11 a/b/g/n/ac/ax
Frequency Band		2412MHz~2484MHz /5170MHZ~5835MHz
Interface		UART/SPI /USB/SDIO
General		
Size		13mm × 26.9 mm ×2.0mm(without shielding cover) 13mm × 26.9 mm ×2.3mm(with shielding cover)
Operating temperature		-20°C ~+80°C
Storage temperature		-40°C ~+85°C
VDD_3V3		3V ~ 3.6V
VDD_IO		1.8V / 3.3V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade		MSL 3
ESD grade		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±400 V, all pins

3. HARDWARE SPECIFICATIONS

3.1 Block Diagram and PIN Diagram

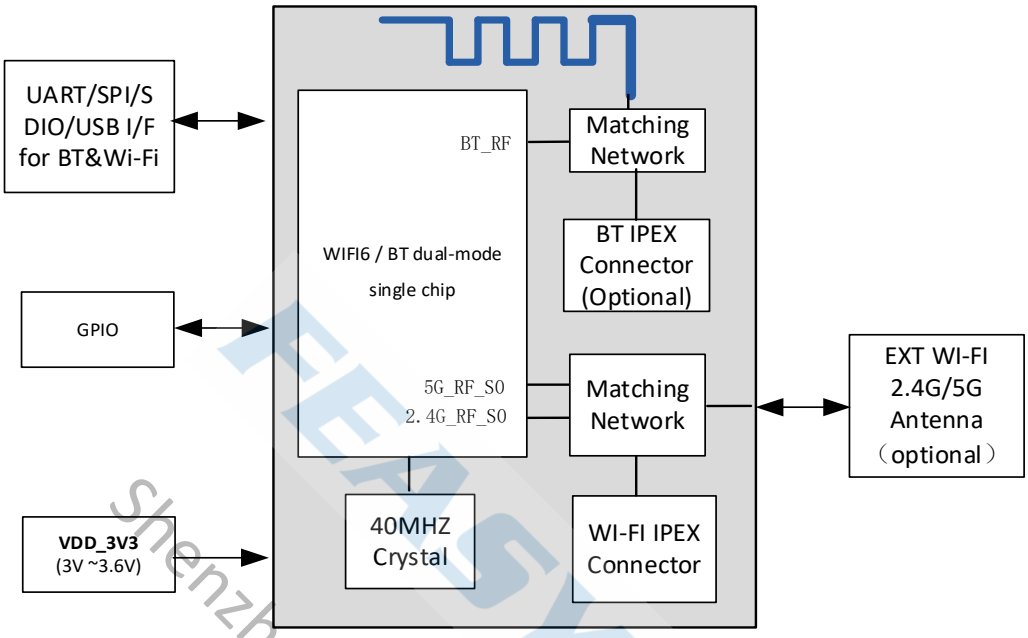


Figure 3-1-1: Block Diagram

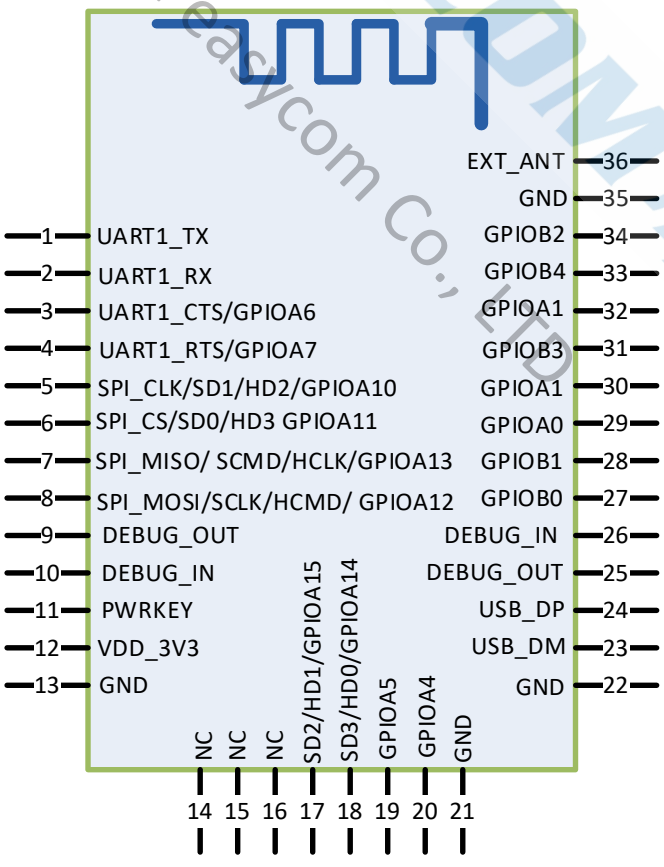


Figure 3-1-2: FSC-BW256B PIN Diagram (Top View)

3.2 Description of PIN Definitions

Table 3-1: Pin definitions

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART1_TX	O	UART Data output	
2	UART1_RX	I	UART Data input	
3	UART1_CTS/GPIOA6	I/O	Programmable input/output line Alternative Function 1: UART Clear to Send (active low)	
4	UART1_RTS/GPIOA7	I/O	Programmable input/output line Alternative Function 1: UART Request to Send (active low)	
5	SPI_CLK/SD1/HD2/ GPIOA10	I/O	SPI_CLK Alternative Function 1: SDIO D1 as slave ; SDIO D2 as master Alternative Function 2: Programmable input/output line	
6	SPI_CS/SD0/HD3/ GPIOA11	I/O	SPI_CS Alternative Function 1: SDIO D0 as slave ; SDIO D3 as master Alternative Function 2: Programmable input/output line	
7	SPI_MISO/ SCMD/HCLK/GPIOA13	I/O	SPI_MISO Alternative Function 1: SDIO CMD as slave ; SDIO CLK as master Alternative Function 2: Programmable input/output line	
8	SPI_MOSI/SCLK/ HCMD/ GPIOA12	I/O	SPI_MOSI Alternative Function 1: SDIO CLK as slave ; SDIO CMD as master Alternative Function 2: Programmable input/output line	
9/25	DEBUG_OUT	I/O	Debug Interface (Data OUT)	
10/26	DEBUG _IN	I/O	Debug Interface (Data IN)	
11	PWRKEY	I	Module power-on pin, power-on = 1; power-off = 0; There is a 47K resistor inside the module, which is pulled up to VDD_3V3	
12	VDD_3V3	VDD	Power supply	
13	GND	VSS	Power Ground	
14	NC			
15	NC			
16	NC			
17	SD2/HD1/GPIOA15	I/O	SDIO D2 as slave ; SDIO D1 as master Alternative Function 1: Programmable input/output line	
18	SD3/HD0/GPIOA14	I/O	SDIO D3 as slave ; SDIO D0 as master Alternative Function 1: Programmable input/output line	
19	GPIOA5	I/O	Programmable input/output line	
20	GPIOA4	I/O	Programmable input/output line	
21	GND	VSS	Power Ground	
22	GND	VSS	Power Ground	
23	USB_DM	I/O	USB data D- Hang in the air when not in use, no need to connect	
24	USB_DP	I/O	USB data D+ Hang in the air when not in use, no need to connect	
27	GPIOB0	I	Programmable input/output line	
28	GPIOB1	I/O	Programmable input/output line	
29	GPIOA0	I/O	Programmable input/output line	
30	GPIOA1	I/O	Programmable input line	
31	GPIOB3	I/O	Programmable input/output line	
32	GPIOA1	I/O	Programmable input/output line	
33	GPIOB4	I/O	Programmable input/output line	
34	GPIOB2	I/O	Programmable input/output line	
35	GND	VSS	RF Ground	

36	EXT_ANT	O	WIFI 2.4G radio frequency WiFi 5G radio frequency（optional）

4. PHYSICAL INTERFACE

4.1 UART Interface

The four signal pins are used to implement the UART function. When FSC-BW256B is connected to another digital device, UART_RX and UART_TX transmit data between the two devices. The remaining two pins UART_CTS and UART_RTS can be used to implement RS232 hardware flow control, and both are low-level effective, that is, transmission is allowed when the level is low, and transmission is stopped when the level is high.

Table 4-1: Possible UART Settings

Parameter	Possible Values	
Baud rate	Minimum	9600bps (≤2%Error)
	Standard	921600bps(≤1%Error)
	Maximum	--
Flow control		RTS/CTS
Parity		None, Odd or Even
Number of stop bits		1 /2
Bits per channel		7/8

When connecting the module to a host, please make sure to follow .

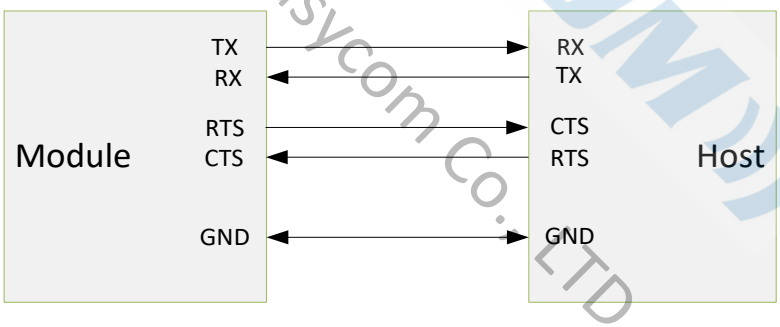


Figure 4-1: UART Connection

5. ELECTRICAL CHARACTERISTICS

5.1 Recommended Operating Conditions

Table 5-1: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3	3	3.3	3.6	V
VDD_IO	1.8	3.3	--	V
Operating temperature (T_A)	-20	27	+80	°C
Storage temperature (T_{stg})	-40	27	+85	°C

High-level input voltage	0.7 X VDD_IO	VDD_IO	V
Low-level input voltage	0	0.3 X VDD_IO	V

5.2 Power Consumption

Table 5-2: Power Consumption :

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VDD_3V3	3.3V	500
VDD_IO	3.3V	-
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW256B Module Power Consumption:

500mA @ VDD_3V3 (Maximum)

Suggest customer design power capacity are 800mA@VDD_3V3 for FSC-BW256B Module.

6. MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30℃/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to simplify manufacturing processes, such as reflow soldering on a PCB. However, Customers are responsible for selecting the appropriate solder paste and confirming that the oven temperatures during reflow meet with the specifications provided by the solder paste manufacturer. Notably, Feasycom surface mount modules adhere to the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

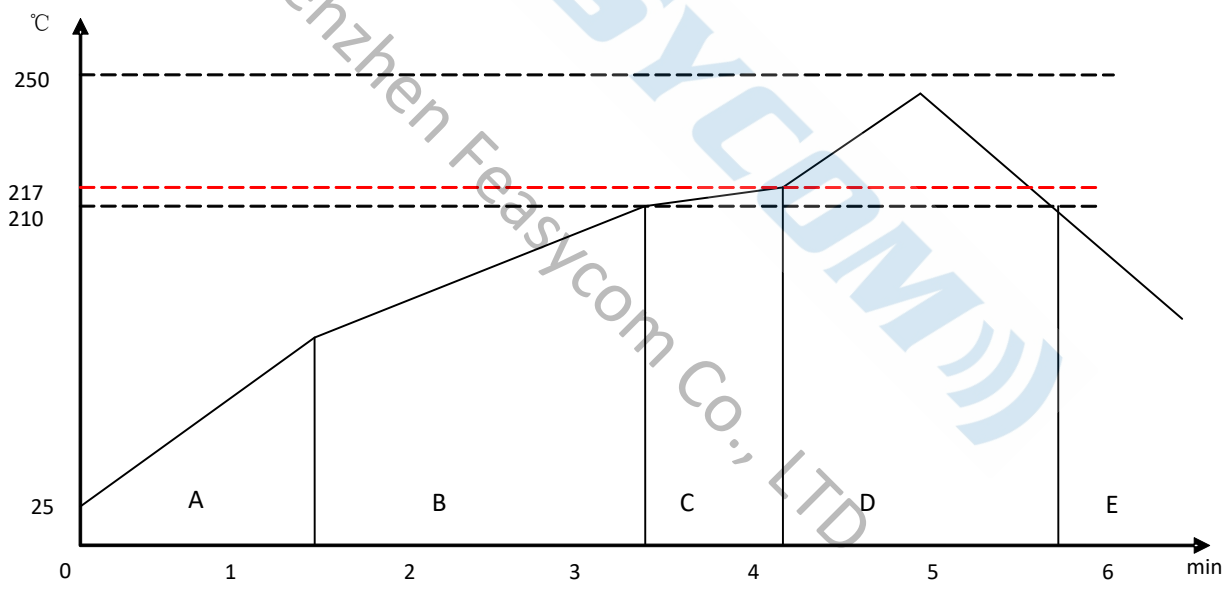


Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate, usually ranging from 0.5 to 2 °C/s. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0mm(H) Tolerance: ±0.2mm(without shielding cover)
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

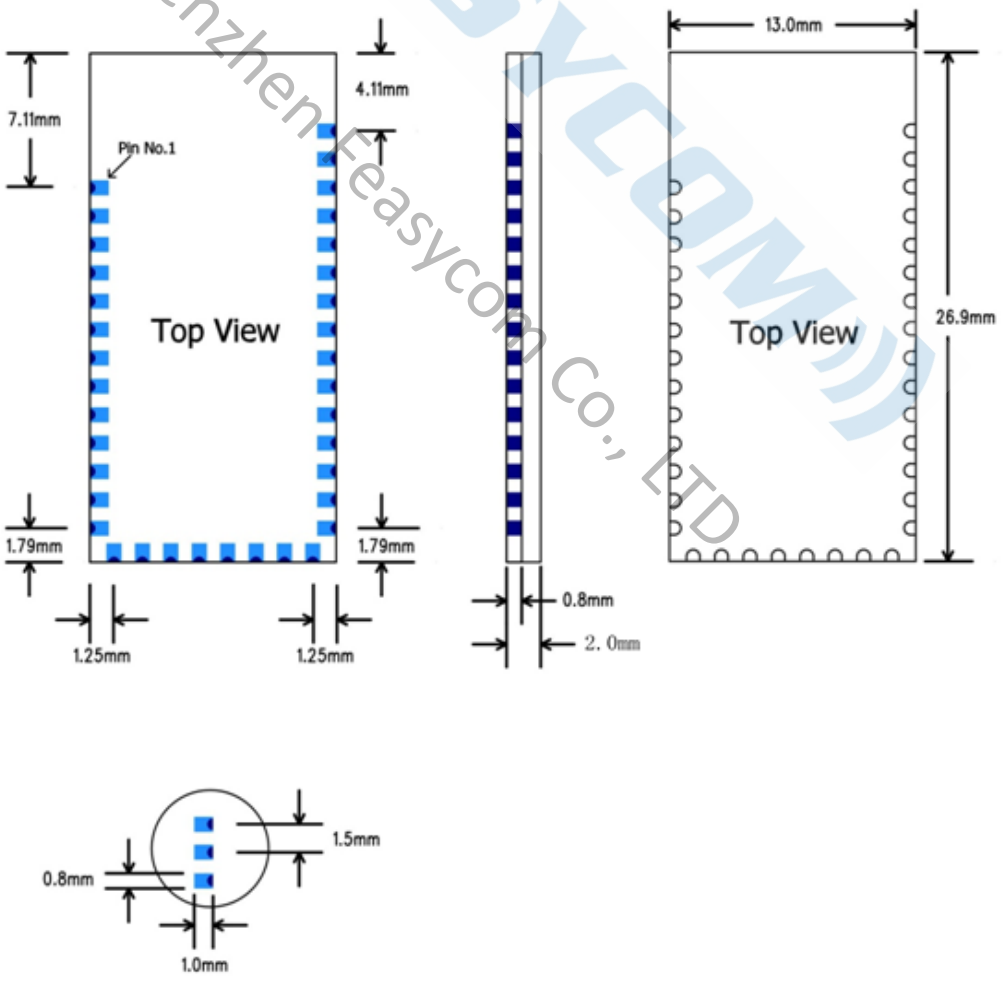


Figure 8-1-1: FSC-BW256B footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

The FSC-BW256B is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to follow good layout practices in order to ensure proper operation of the module. Placing copper or any metal near the antenna can negatively impact its performance by affecting the matching properties. To prevent radiation, a metal shield should not be used with the module. It is advised to use grounding vias, spaced a maximum of 3 mm apart, at the edge of grounding areas to prevent RF penetration inside the PCB and unintentional resonator formation. Additionally, GND vias should be distributed all around the PCB edges.

In the restricted area where the on-board antenna is located, the motherboard should not have any bare conductors or vias. This area is not covered by stop mask print, so no copper (planes, traces, or vias) should be present in this area to avoid mismatching with the on-board antenna.

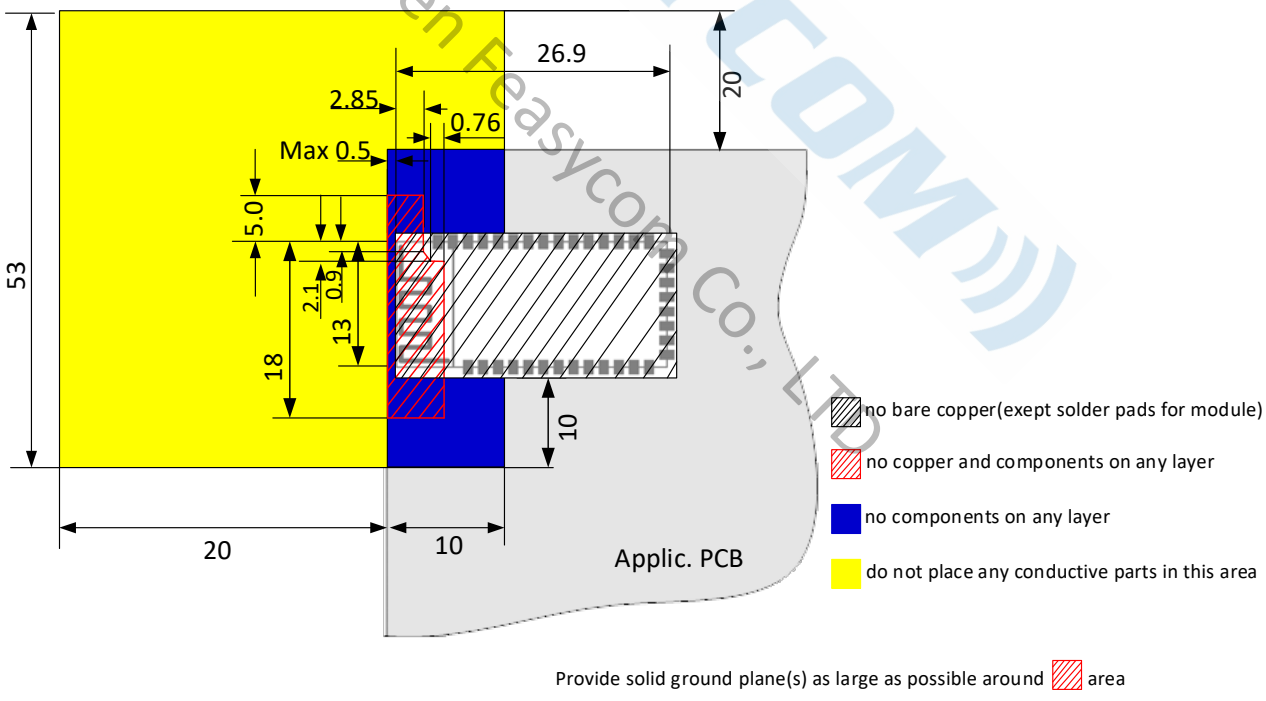


Figure 9-2-1: Restricted Area (Design schematic, for reference only. Unit: mm)

The provided recommendations target the prevention of EMC issues stemming from the RF component of the module. It is crucial to recognize the uniqueness of each design, with this list not encompassing all fundamental design principles, such as mitigating capacitive coupling between signal lines. Moreover, it is essential to address potential challenges posed by digital signals in the design process.

To address EMC concerns effectively, it is recommended to keep the return paths of signal lines as short as feasible. For instance, when a signal traverses a via to an inner layer, always use ground vias around it. These ground vias should be

positioned closely and symmetrically around the signal vias. Routing of delicate signals is best done within the inner layers of the PCB. Sensitive traces should be flanked by ground planes both above and below the line. If this arrangement is not viable, ensure a short return path by exploring alternative techniques, like situating a ground line adjacent to the signal line.

9.3 Layout Guidelines(External Antenna)

The placement and layout of the PCB are vital in enhancing the performance of modules without on-board antenna designs. The trace linking the antenna port of the module to an external antenna should maintain a characteristic impedance of 50Ω and be kept as brief as feasible to prevent interference with the module's transceiver. When situating the external antenna and RF-IN port of the module, it is crucial to isolate them from potential sources of noise and digital traces. To reduce return loss and attain improved impedance matching, a matching network might be necessary between the external antenna and RF-IN port.

For optimal RF performance, it is advised to distinctly segregate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are positioned in proximity to the antenna port. Therefore, when placing the module, the digital part of the module should face the digital part of the system PCB.

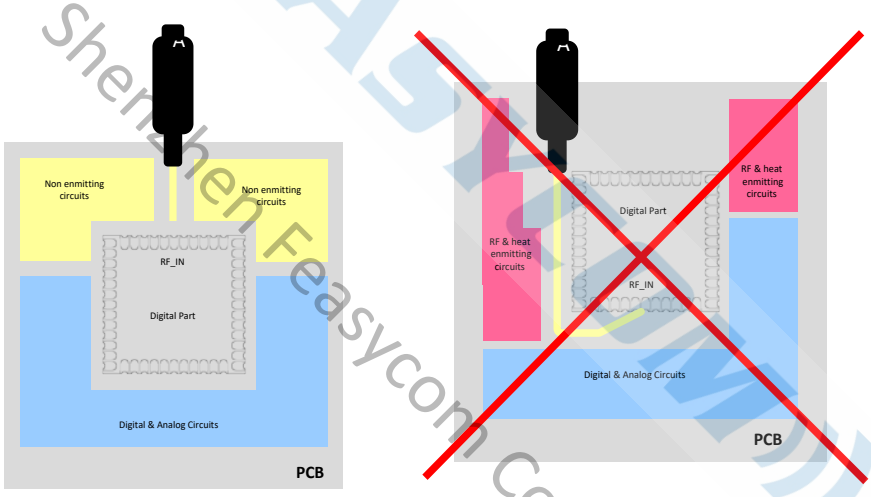


Figure 9-3-1: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

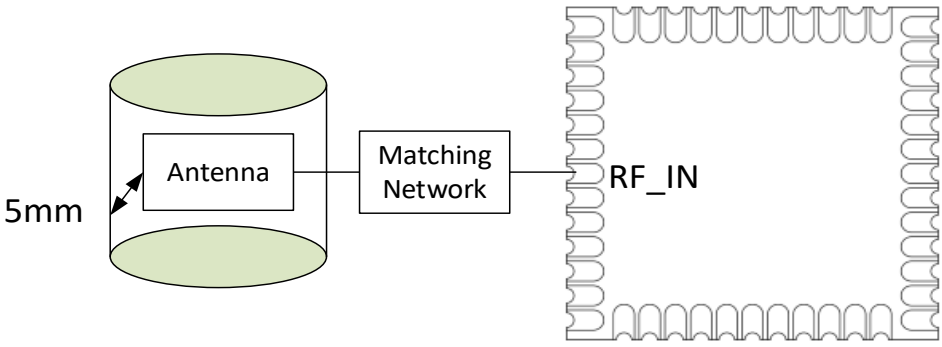


Figure 9-3-1-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

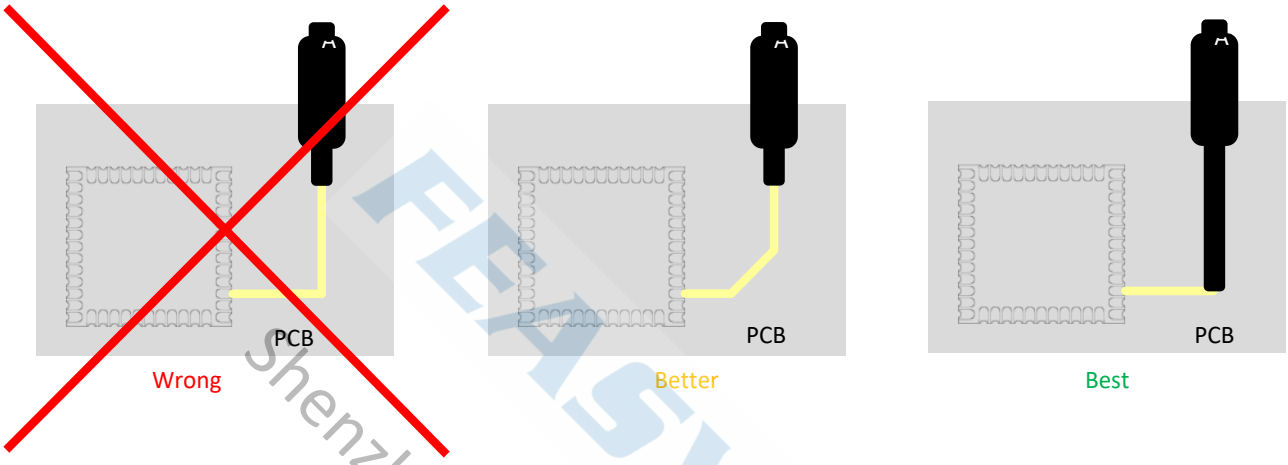


Figure 9-3-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD_WL

SDIO_CLK_WL

SDIO_D0_WL ~ SDIO_D3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

HCI_RX_BT

HCI_TX_BT

HCI_CTS_BT

HCI_RTS_BT

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

9.7 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW256B Module Ground Pads

Decoupling Capacitors close to FSC-BW256B Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 10-1-1: Tray vacuum

10.2 Packing box(Optional)

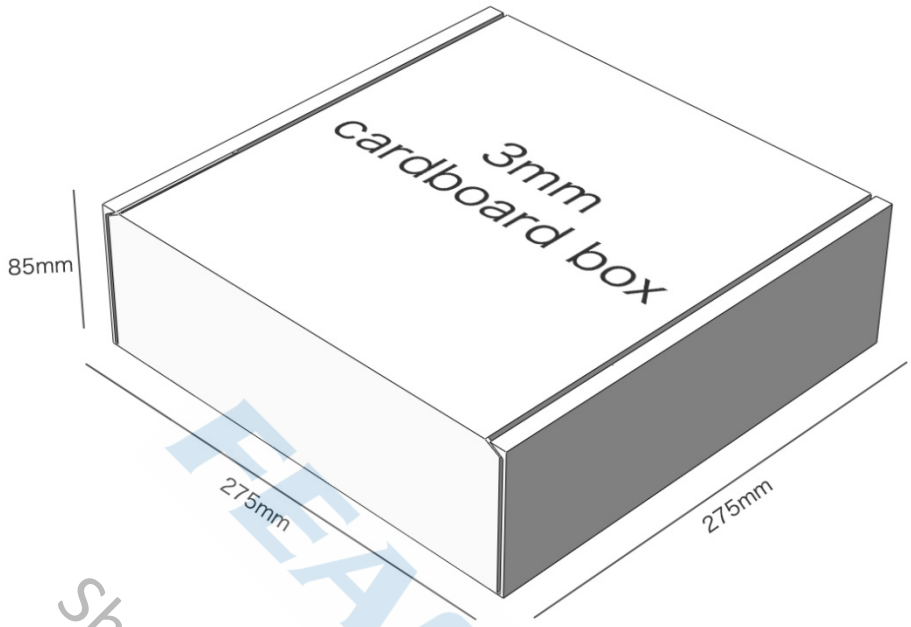


Figure 10-2-1: Packing box

* If any packaging other than the package mentioned above is required, please confirm the packaging size again.
* Packing: 1000pcs per carton (Minimum packing quantity).
* The outer packing size provided above is for reference purposes only. For the actual dimensions of the product's pack aging, please refer to the packaging of the actual goods.

11. APPLICATION SCHEMATIC