FSC-BW8201SI

Bluetooth 5.2 + Dual-band 1x1 802.11n Module Datasheet

Version 1.0

Revision History

Version	Data	Notes	Approved By
1.0	2024/05/31	Initial Version	guangxian Ma

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1. INTRODUCTION

Overview

The FSC-BW8201SI is a compact and low-profile Wi-Fi + Bluetooth Combo module with LGA module, board size is 23.4*19.4mm. With a board size of just 23.4mm x 19.4mm, it is ideal for integration into tablet PCs, mobile devices, and various consumer products. The module is designed for easy manufacturing using the SMT (Surface-Mount Technology) process.It provides SDIO 2.0 interface for Wi-Fi to connect with host processor. It also includes a high-speed UART interface for Bluetooth 5.2, ensuring robust and efficient communication. Additionally, the module features a PCM (Pulse Code Modulation) interface for audio data transmission, enabling a direct link to external audio codecs via the Bluetooth controller.

The Wi-Fi throughput can theoretically reach up to 150 Mbps using 802.11n technology.

General Features

- Operate at 2.4G&5GHz frequency bands
- 802.11b/g/n/a + Bluetooth V2.1+EDR and BT5.2
- Enterprise level security which can apply WPA/WPA2/WPA3
- Wi-Fi 1T1R allow data rates supporting up to 150 Mbps PHY rates

Host Interface

- SDIO2.0 for Wi-Fi and UART for BT5.2
- PCM interface for audio data transmission via BT controller

Bluetooth Features

- Compatible with Bluetooth v2.1+EDR and V5.2 system
- Support BT5.2 dual mode

Applications

- Audio and video system
- Measurement systems
- PND

Module picture as below showing

Figure 1: FSC-BW8201SI Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
General		
	Model Name	FSC-BW8201SI
	Product Description	Support Wi-Fi/Bluetooth functionalities
	Dimension	23.4 x 19.4 x2.6 mm
	Wi-Fi Interface	Support SDIO V1.1/2.0
	BT Interface	UART
	Operating temperature	-40°C ~ +85°C
	Storage temperature	-40°C ~ +85°C
	Supply Voltage	3.2V~3.6V
	Miscellaneous	Lead-free and RoHS compliant One Year
	Humidity	10% ~ 90% non-condensing
	MSL grade:	MSL 3
	ESD grade:	Human Body Model: Pass ±3500 V, all pins Charge device model: Pass ±500 V, all pins
Bluetooth		
	Bluetooth Standard	Bluetooth V5.2+EDR
	Frequency Band	2402MHz~2480MHz
	Transmit power	9dBm (Max.)
	Receiver sensitivity	-92dBm (Max.)
	Profiles	HFP, A2DP, AVRCP, PBAP, SPP, HID, BLE
Wi-Fi 2.4GHz		
	WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant
	Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
	Number of Channels	2.4GHz：Ch1 ~ Ch14
	Output Power	802.11b /11Mbps : 17dBm ± 2 dB EVM≤-9dB 802.11g /54Mbps : 15dBm ± 2 dB EVM≤-25dB 802.11n /MCS7: 14dBm ± 2 dB EVM≤-28dB
	Spectrum Mask	Meet with IEEE standard
	Freq. Tolerance	±20ppm
	SISO Receive Sensitivity (11b,20MHz) @8% PER	1Mbps PER @ -92dBm EVM≤-83 2Mbps PER @ -90dBm EVM≤-80 5.5Mbps PER @ -87dBm EVM≤-79 11Mbps PER @ -85dBm EVM≤-76
	SISO Receive Sensitivity (11g,20MHz) @10% PER	6Mbps PER @ -89dBm EVM≤-85 9Mbps PER @ -88dBm EVM≤-84 12Mbps PER @ -87dBm EVM≤-82

		18Mbps	PER @ -84dBm	EVM≤-80
		24Mbps	PER @ -81dBm	EVM≤-77
		36Mbps	PER @ -78dBm	EVM≤-73
		48Mbps	PER @ -73dBm	EVM≤-69
		54Mbps	PER @ -71dBm	EVM≤-68
	SISO Receive Sensitivity (11n,20MHz) @10% PER	MCS=0	PER @ -89dBm	EVM≤-85
		MCS=1	PER @ -86dBm	EVM≤-82
		MCS=2	PER @ -84dBm	EVM≤-80
		MCS=3	PER @ -80dBm	EVM≤-77
		MCS=4	PER @ -77dBm	EVM≤-73
		MCS=5	PER @ -72dBm	EVM≤-69
		MCS=6	PER @ -71dBm	EVM≤-68
		MCS=7	PER @ -69dBm	EVM≤-67
	SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0	PER @ -88dBm	EVM≤-82
		MCS=1	PER @ -85dBm	EVM≤-79
		MCS=2	PER @ -83dBm	EVM≤-77
		MCS=3	PER @ -79dBm	EVM≤-74
		MCS=4	PER @ -76dBm	EVM≤-70
		MCS=5	PER @ -71dBm	EVM≤-66
		MCS=6	PER @ -70dBm	EVM≤-65
		MCS=7	PER @ -68dBm	EVM≤-64
	Maximum Input Level	802.11b : -10dBm 802.11g/n : -20dBm		
	Antenna Reference	Small antennas with 0~2dBi peak gain		
Wi-Fi 5GHz				
	WLAN Standard	IEEE 802.11a/n Wi-Fi compliant		
	Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)		
	Number of Channels	5.0GHz: 36,40,44,48; 52,56,60,64; 100,104,108,112,116,120,124,128,132,136,140; 149,153,157,161,165.		
	Output Power	802.11a/54Mbps: 15dBm ± 2dB		EVM≤-25dB
		802.11n /MCS7: 14dBm ± 2 dB		EVM≤-28dB
	SISO Receive Sensitivity (11a,20MHz) @10% PER	6Mbps	PER @ -88dBm	EVM≤-85
		9Mbps	PER @ -87dBm	EVM≤-84
		12Mbps	PER @ -86dBm	EVM≤-82
		18Mbps	PER @ -83dBm	EVM≤-80
		24Mbps	PER @ -80dBm	EVM≤-77
		36Mbps	PER @ -77dBm	EVM≤-73
		48Mbps	PER @ -72dBm	EVM≤-69
		54Mbps	PER @ -70dBm	EVM≤-68
	SISO Receive Sensitivity (11n,20MHz) @10% PER	MCS=0	PER @ -88dBm	EVM≤-85

	MCS=1	PER @ -85dBm	EVM≤-82
	MCS=2	PER @ -83dBm	EVM≤-80
	MCS=3	PER @ -80dBm	EVM≤-77
	MCS=4	PER @ -76dBm	EVM≤-73
	MCS=5	PER @ -71dBm	EVM≤-69
	MCS=6	PER @ -70dBm	EVM≤-68
	MCS=7	PER @ -69dBm	EVM≤-67
SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0	PER @ -85dBm	EVM≤-82
	MCS=1	PER @ -82dBm	EVM≤-79
	MCS=2	PER @ -80dBm	EVM≤-77
	MCS=3	PER @ -77dBm	EVM≤-74
	MCS=4	PER @ -73dBm	EVM≤-70
	MCS=5	PER @ -69dBm	EVM≤-66
	MCS=6	PER @ -68dBm	EVM≤-65
	MCS=7	PER @ -67dBm	EVM≤-64
Maximum Input Level	802.11a/n : -30dBm		
Antenna Reference	Small antennas with 0~2dBi peak gain		

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

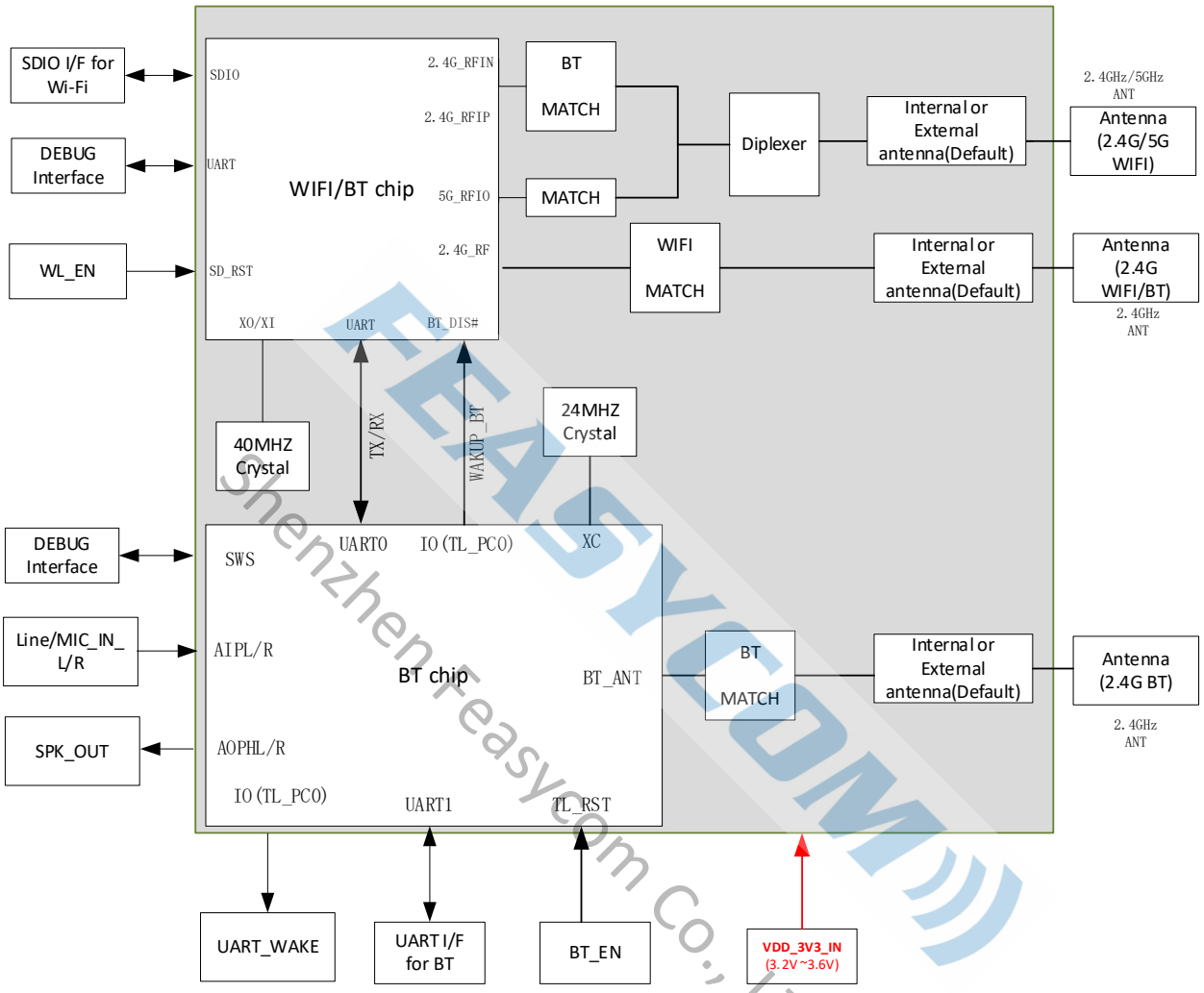


Figure 2: Block Diagram

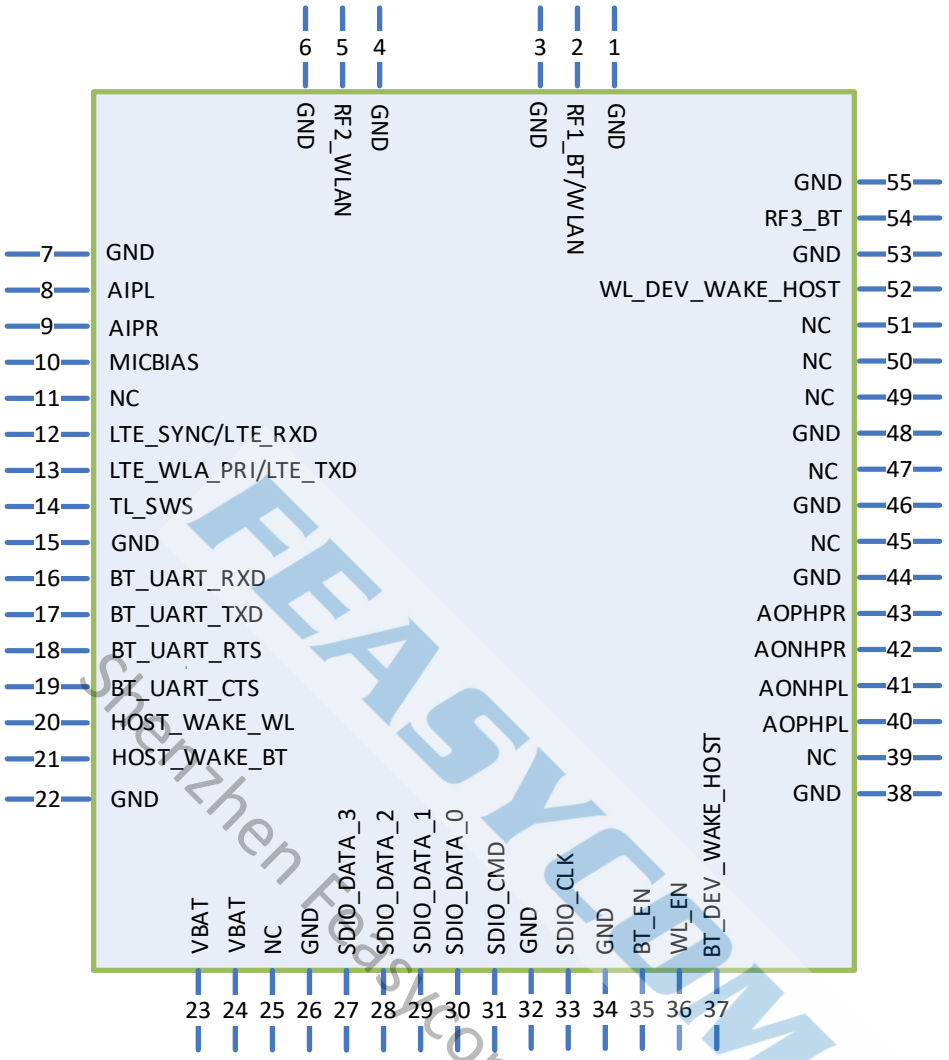


Figure 3: FSC-BW8201SI PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND		Ground	
2	RF1_BT/WLAN	RF	WLAN 2.4 GHz and Bluetooth RF input/output port	
3	GND		Ground	
4	GND		Ground	
5	RF2_WLAN	RF	WLAN 2.4/5GHz RF input/output port	
6	GND		Ground	
7	GND		Ground	
8	AIPL	Analog	Left channel single-ended or positive analog input	
9	AIPR	Analog	Right channel single-ended or positive analog input	
10	MICBIAS	Analog	Microphone biasing voltage	

11	NC		
12	LTE_SYNC/LTE_RXD	I/O	LTE co-existence signal. LTE_UART_RXD or LTE_FS. NC if not used.
13	LTE_WLA_PRI/LTE_TXD	I/O	LTE co-existence signal. LTE_UART_TXD or LTE_PRI. NC if not used.
14	TL_SWS	I/O	Programmable I/O Alternative function: DEBUG Interface
15	GND		Ground
16	BT_UART_RXD	I	BT UART I/F
17	BT_UART_TXD	O	BT UART I/F
18	BT_UART_RTS	I/O	BT UART I/F
19	BT_UART_CTS	I/O	BT UART I/F
20	HOST_WAKE_WL	I	Host wakeup WL; active high. NC if not used.
21	HOST_WAKE_BT	I	Host wakeup Bluetooth; active high. NC if not used.
22	GND		Ground
23	VBAT	PWR	3.3V Supply Voltage
24	VBAT	PWR	3.3V Supply Voltage
25	NC		
26	GND		Ground
27	SDIO_DATA_3	I/O	SDIO data bus D3
28	SDIO_DATA_2	I/O	SDIO data bus D2
29	SDIO_DATA_1	I/O	SDIO data bus D1
30	SDIO_DATA_0	I/O	SDIO data bus D0
31	SDIO_CMD	I	SDIO command signal
32	GND		Ground
33	SDIO_CLK	I	SDIO clock signal
34	GND		Ground
35	BT_EN	I	Bluetooth Function Enable(High Active)(BT Reset)
36	WL_EN	I	Wi-Fi Function Enable(High Active) (Wi-Fi Reset)
37	BT_DEV_WAKE_HOST	O	Bluetooth wakeup the host; active high. NC if not used.
38	GND		Ground
39	NC		
40	AOPHPL	Analog	Left channel positive headphone output
41	AONHPL	Analog	Left channel negative headphone output
42	AONHPR	Analog	Right channel negative headphone output
43	AOPHPR	Analog	Right channel positive headphone output
44	GND		Ground
45	NC		
46	GND		Ground
47	NC		
48	GND		Ground
49	NC		
50	NC		

51	NC		
52	WL_DEV_WAKE_HOST	O	WL wakeup the host; active high. NC if not used.
53	GND		Ground
54	RF3_BT	RF	Bluetooth RF input/output port
55	GND		Ground

PWR= Power Input(3.2V~3.6V); I/O=Bi-directional(3.2V~3.6V); I=Input; O=Output; RF=RF Pin; GND=Ground; F=Floating (Not Connected)

5. MSL & ESD

Table 3: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – ESD_HAND_HBM - Human body model contact discharge per JEDEC EID/JESD22-A114F-2008	Pass ±35000 V, all pins
ESD – ESD_HAND_CDM - Charged device model contact discharge per JEDEC EIA/JESD22-C101F-2013	Pass ±500 V, all pins

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 4: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

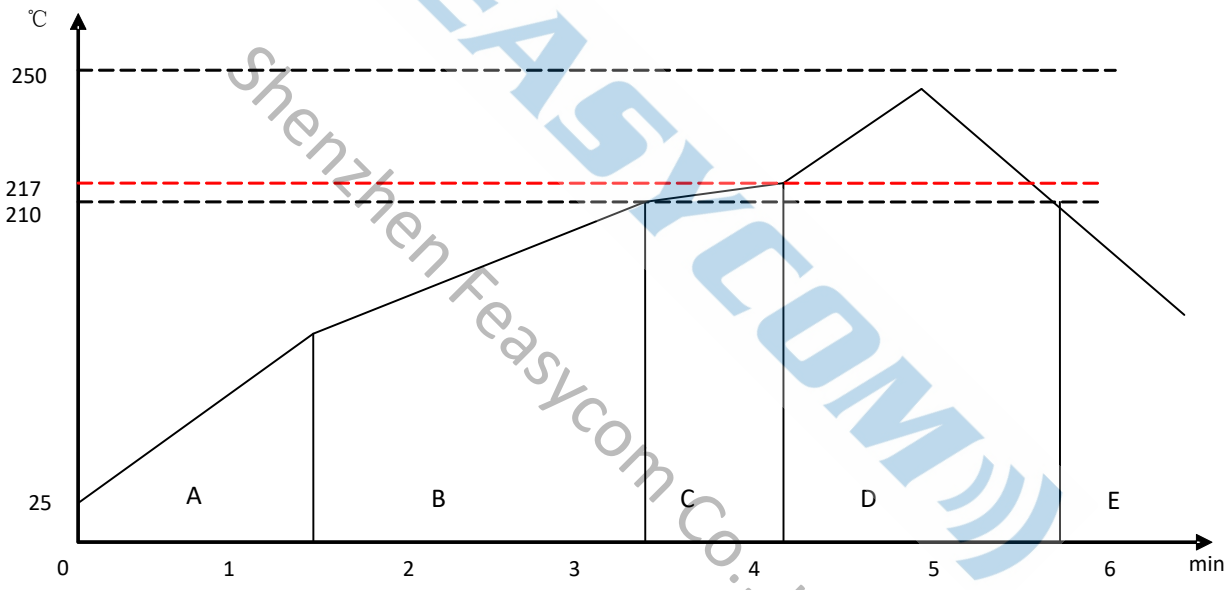


Figure 4: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the

temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

7. MECHANICAL DETAILS

7.1 Mechanical Details

- Dimension: 23.4mm(L) x 19.4mm(W) x 2.6mm(H) Tolerance: ±0.1mm
- Module size: 23.4mm x 19.4mm Tolerance: ±0.25mm
- Pad size: 2mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1) 1.4mm ±0.1mm 2) 1.2mm ±0.1mm 3) 1.1mm ±0.1mm

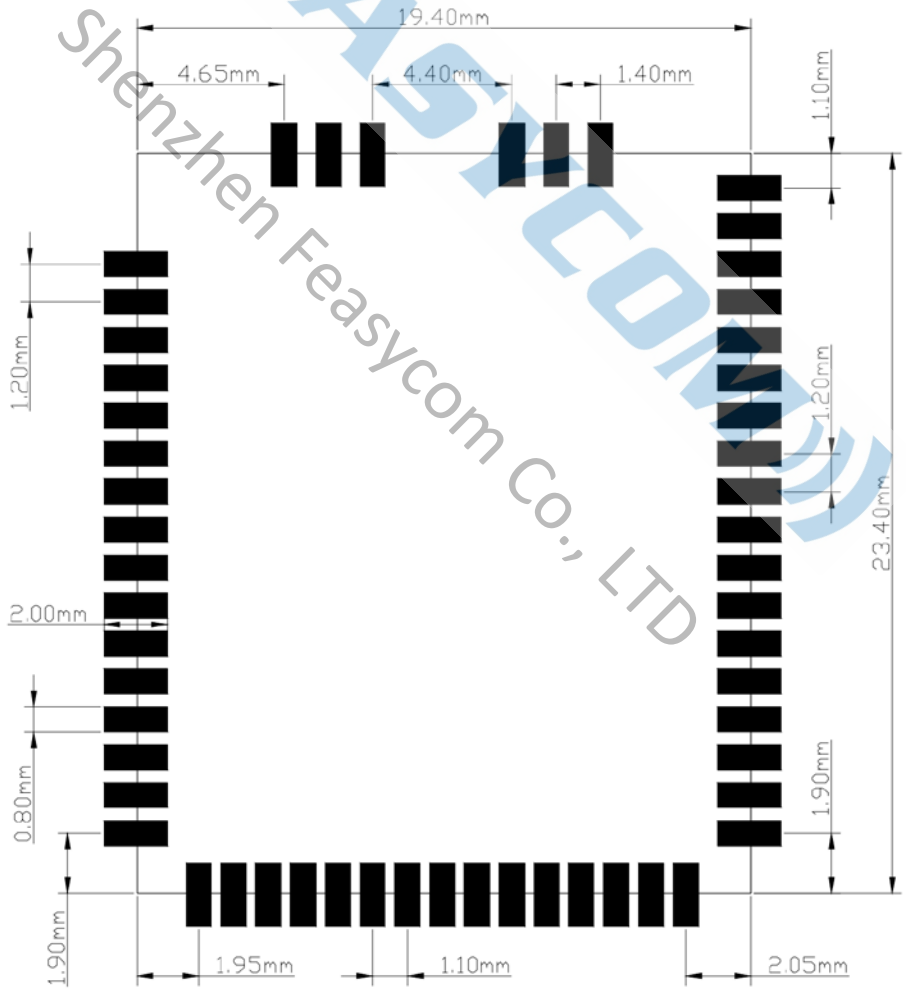


Figure 5: FSC-BW8201SI footprint Layout Guide (Top View)

8. HARDWARE INTEGRATION SUGGESTIONS

8.1 Connections when BT's HCI is by UART

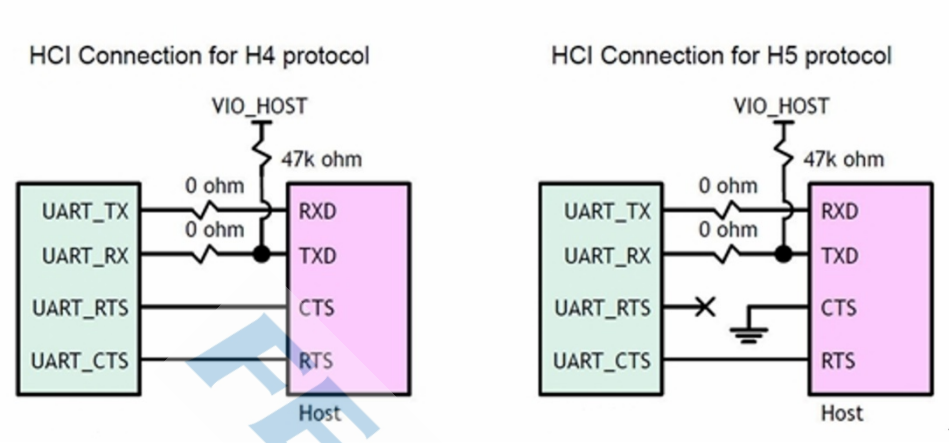


Figure 6: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.

   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)

2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

8.2 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

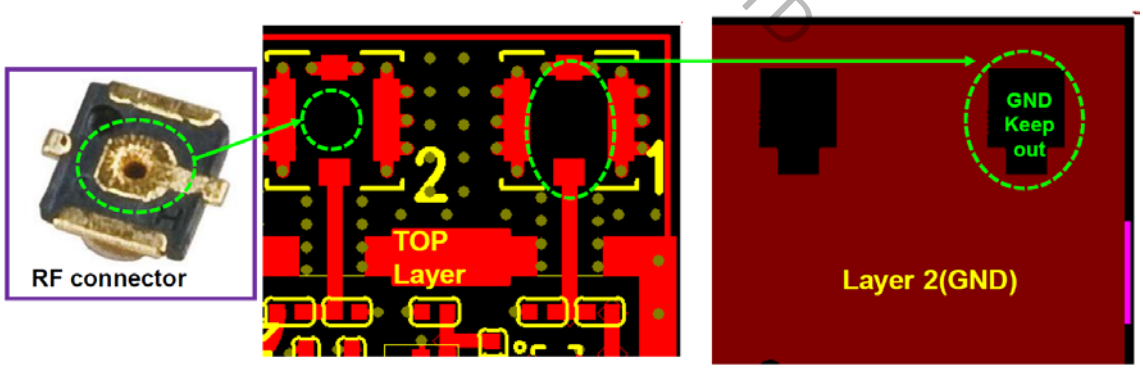


Figure 7: RF Circuit- RF pads

8.3 Recommendable antenna & IPEX by Feasycom

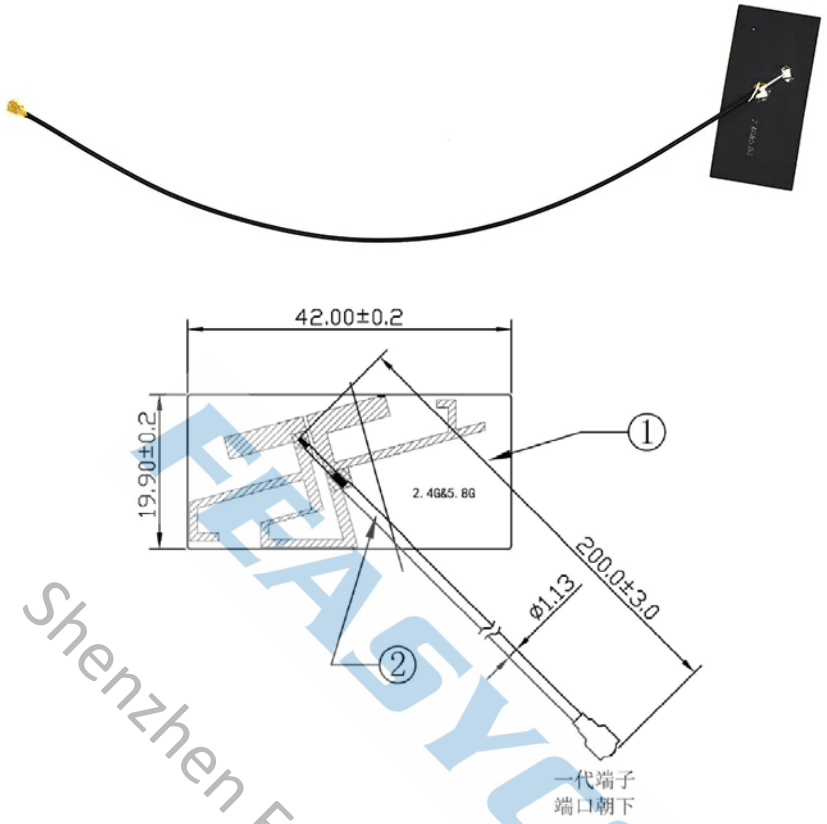


Figure 8: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface

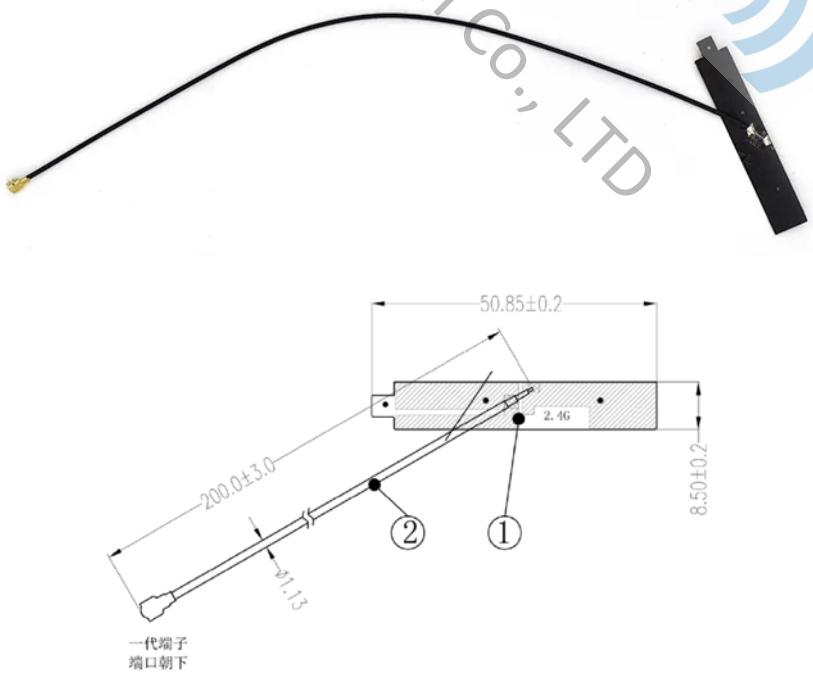


Figure 9: 2.4GHz antenna with IPEX first generation interface

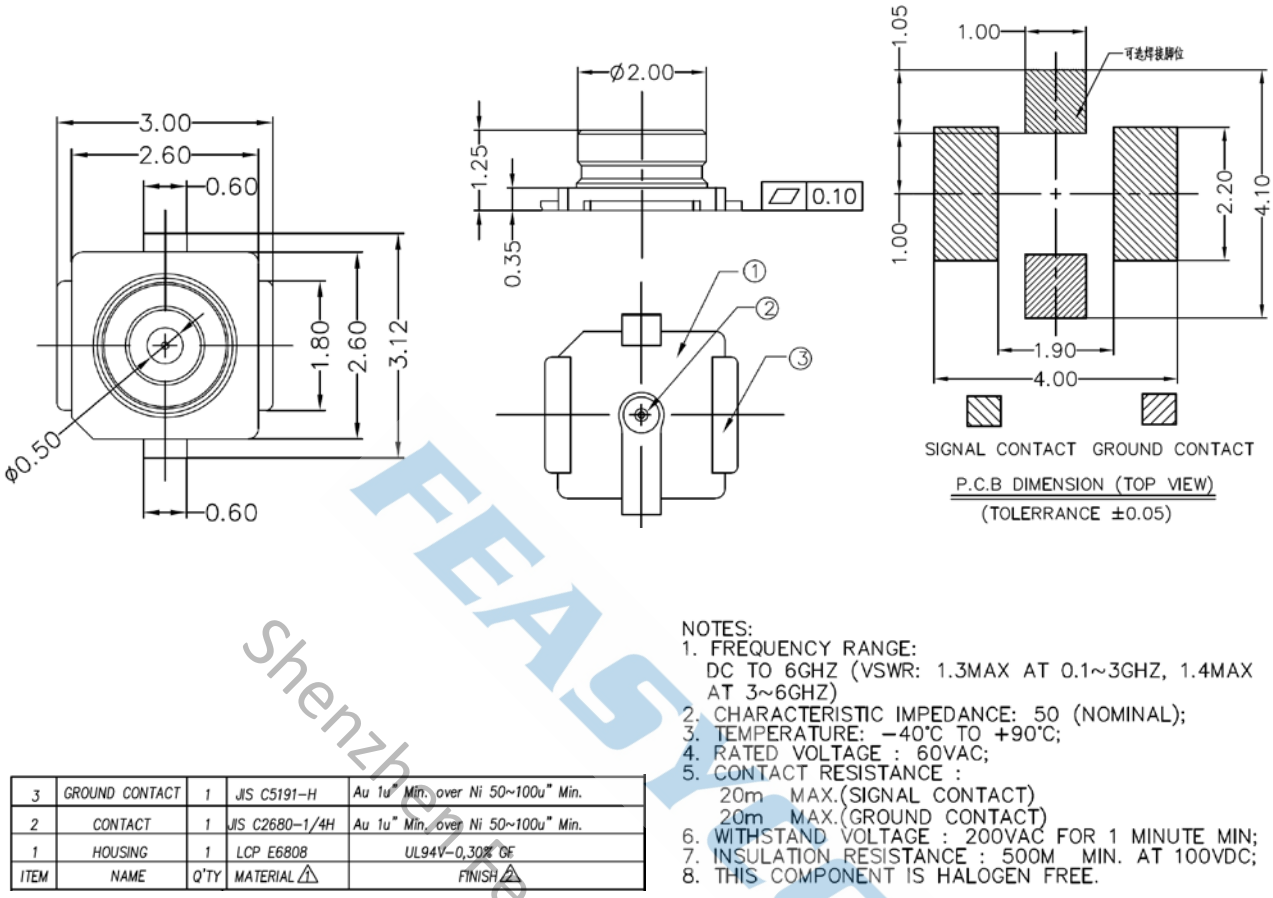


Figure 10: IPEX first generation interface

8.4 Soldering Recommendations

The FSC-BW8201SI module is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile can vary based on factors such as the thermal mass of the populated PCB, the heat transfer efficiency of the oven, and the type of solder paste used. It is recommended to consult the datasheet of the specific solder paste for precise profile configurations.

Feasycom provides the following soldering recommendations to ensure reliable solder joints and optimal module performance. However, since the ideal profile may differ depending on the unique process and layout, these suggestions should be considered as initial guidance. A thorough analysis of the specific scenario is advised to achieve the best results.

8.5 Layout Guidelines(Internal Antenna)

Adherence to sound layout practices is highly recommended to guarantee the module's correct operation. Placing copper or any metal in close proximity to the antenna can detrimentally affect its performance by interfering with the matching properties. To avoid radiation issues, refrain from using a metal shield with the module. It is advisable to incorporate grounding vias, spaced no more than 3 mm apart, along the periphery of grounding areas to inhibit RF penetration within the PCB and prevent unintended resonator formation. Furthermore, ensure that GND vias are evenly dispersed along all edges of the PCB.

In the restricted area where the on-board antenna is located, the motherboard should not have any bare conductors or vias. This area is not covered by stop mask print, so no copper (planes, traces, or vias) should be present in this area to

avoid mismatching with the on-board antenna.

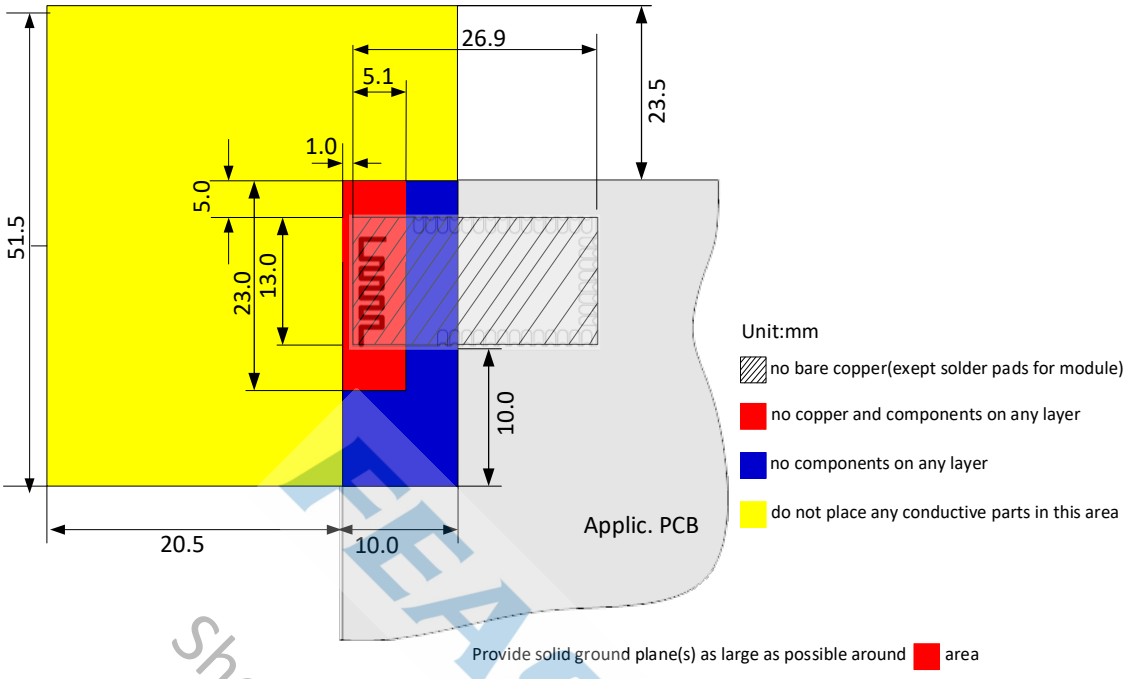


Figure 11: Restricted Area (Reference design) Unit: mm

The provided recommendations target the prevention of EMC issues stemming from the RF component of the module. It is crucial to recognize the uniqueness of each design, with this list not encompassing all fundamental design principles, such as mitigating capacitive coupling between signal lines. Moreover, it is essential to address potential challenges posed by digital signals in the design process.

To address EMC concerns effectively, it is recommended to keep the return paths of signal lines as short as feasible. For instance, when a signal traverses a via to an inner layer, always use ground vias around it. These ground vias should be positioned closely and symmetrically around the signal vias. Routing of delicate signals is best done within the inner layers of the PCB. Sensitive traces should be flanked by ground planes both above and below the line. If this arrangement is not viable, ensure a short return path by exploring alternative techniques, like situating a ground line adjacent to the signal line.

8.6 Layout Guidelines(External Antenna)

The placement and layout of the PCB are vital in enhancing the performance of modules without on-board antenna designs. The trace linking the antenna port of the module to an external antenna should maintain a characteristic impedance of 50Ω and be kept as brief as feasible to prevent interference with the module's transceiver. When situating the external antenna and RF-IN port of the module, it is crucial to isolate them from potential sources of noise and digital traces. To reduce return loss and attain improved impedance matching, a matching network might be necessary between the external antenna and RF-IN port.

For optimal RF performance, it is advised to distinctly segregate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are positioned in proximity to the antenna port. Therefore, when placing the module, the digital part of the module should face the digital part of the system PCB.

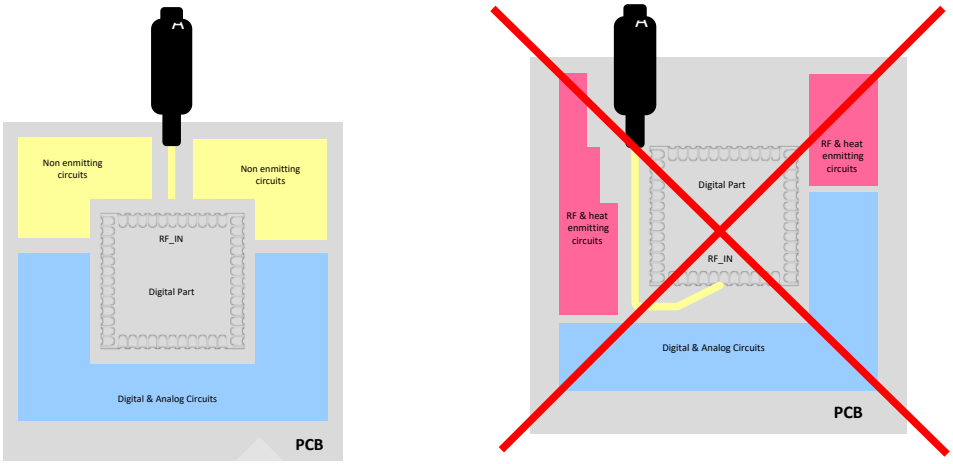


Figure 12: Placement the Module on a System Board

8.6.1 Antenna Connection and Grounding Plane Design

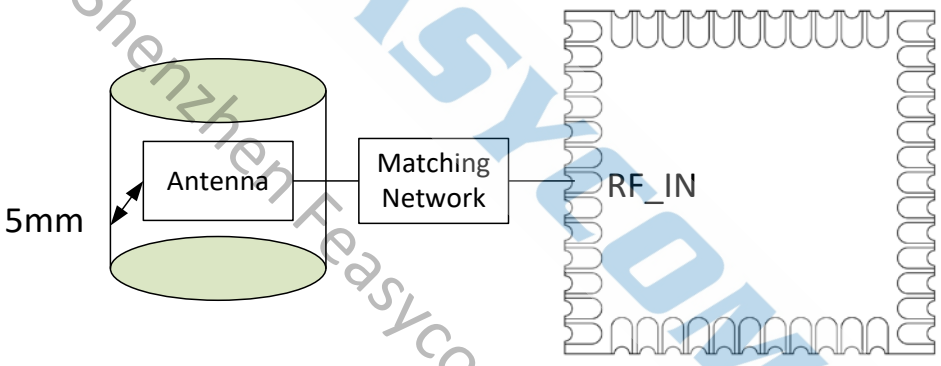


Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

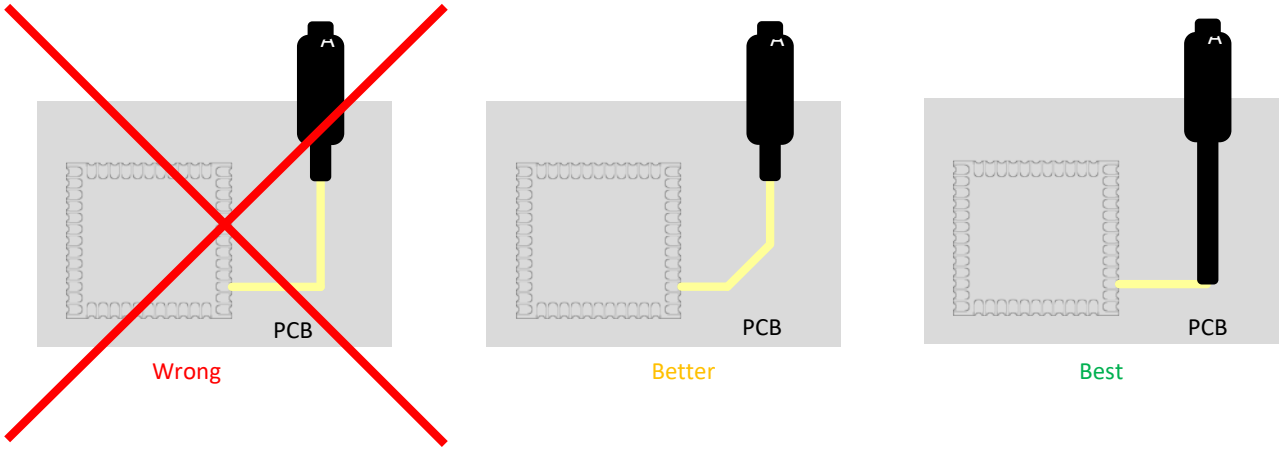


Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9. PRODUCT PACKAGING INFORMATION

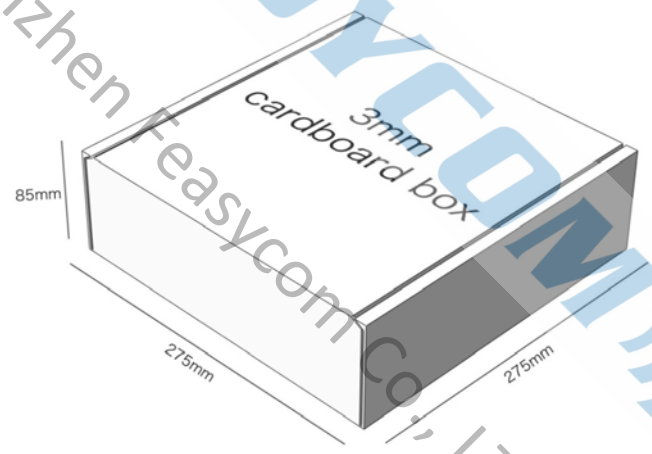
9.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 140mm * 265mm

Figure 15: Tray vacuum

9.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 500PCS Per Carton (Min Carton Package)

Figure 16: Packing Box

10. APPLICATION SCHEMATIC