FSC-BT836B

5.3 Dual Mode Bluetooth Module Data Sheet

Document Type: FSC-BT836B

Document Version: V2.51

Release Date: May 14. 2024

Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District, Shenzhen, 518102, China
Tel: 86-755-27924639

Release Record

Version Number	Release Date	Comments
Revision 2.0	2019-08-17	First Release
Revision 2.1	2019-11-16	Update antenna package
Revision 2.2	2020-04-30	Increase power consumption parameters
Revision 2.3	2020-05-10	Modify humidity
Revision 2.4	2020-07-20	Increase chip model
Revision 2.5	2023-08-11	Update operating temperature -20ºC to +85 ºC, Bluetooth version V5.3
Revision 2.51	2024-05-14	Added operating temperature: 0ºC to +70 ºC

1. INTRODUCTION

FSC-BT836B is Feasycom's dual-mode (BR/EDR and LE) Bluetooth 5.3 compliant module. It supports SPP, HID, GATT, ATT, and other profiles. It provides several customizable hardware interfaces such as UART, USB, PCM, I2C, AIO, PIO, etc.

FSC-BT836B incorporates high-performance MCU, Bluetooth controller and chip antenna in a small package so that customers can integrate FSC-BT836B in small products.

FSC-BT836B uses UART as the programming interface, customers can use AT commands to read or write the configuration of the module through UART. FSC-BT836B is powered by Feasycom's Bluetooth stack which could provide more possibilities to the applications of customers. For programming with FSC-BT836B, please refer to the relevant programming user guide.

1.1 Block Diagram

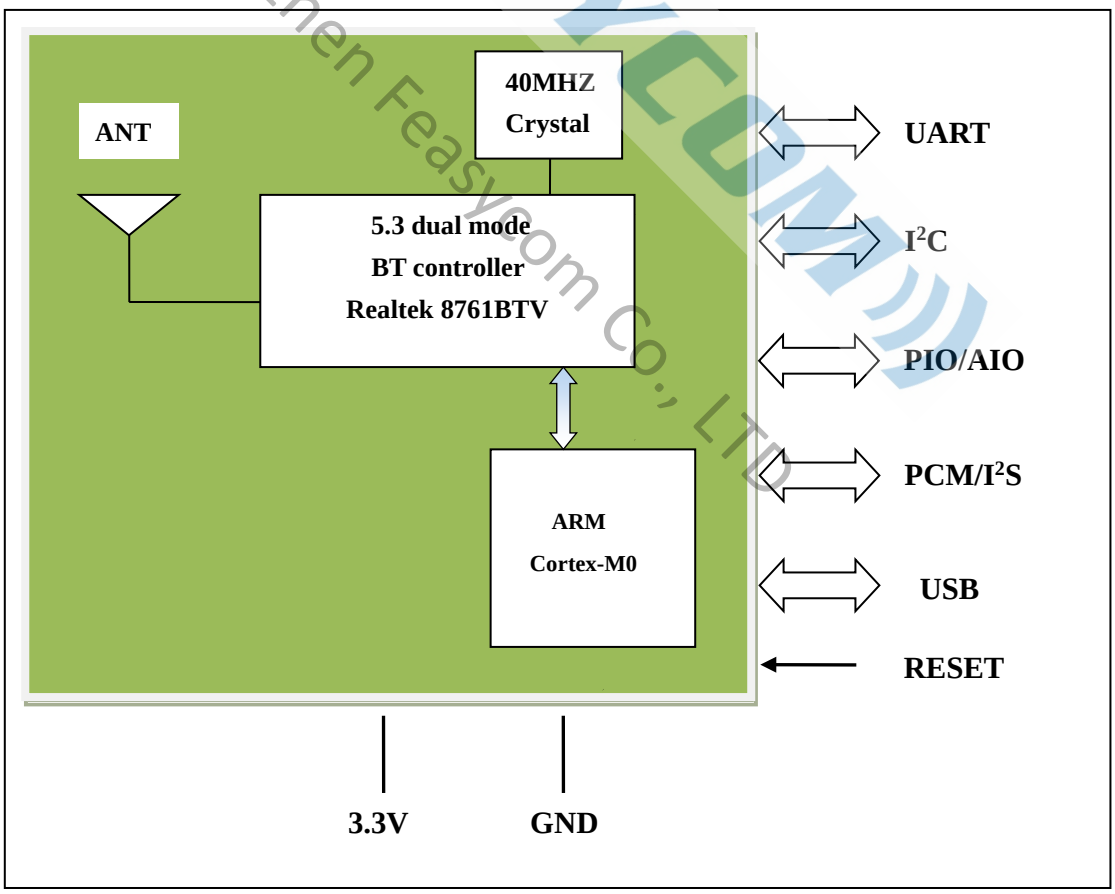

Figure 1

1.2 Feature

- Fully qualified Bluetooth 5.3/4.2/4.0/3.0/2.1/2.0/1.2/1.1
- Postage stamp sized form factor
- Low power
- Supports TX +10dBm maximum output power for Bluetooth BR/BLE

  Supports TX +7.5dBm maximum output power for Bluetooth EDR
- Receive sensitivity: -94 dBm(2Mbps EDR Minimum)

  -98 dBm(BLE Minimum)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921.6Kbps
- UART, I²C ,USB hardware interfaces
- Support the OTA upgrade
- Embedded Bluetooth stack profiles support: SPP, HID,GATT, ATT, GAP
- Support iBeacon
- Power Consumption In Sleep Mode (VDD_3V3 at 3.3 V)
  - Discoverable：2.5mA
  - BR/EDR Connection：9.89mA
  - LE Connection：6.15mA
- Power Consumption In Working Mode (VDD_3V3 at 3.3 V)
  - Discoverable：21.75mA
  - BR/EDR Connection：24.92mA
  - LE Connection：20.79mA
  - BR/EDR Connection @ 115200bps：25.11mA

1.3 Applications

- Smart Watch and Bluetooth Bracelet
- Health & Medical devices
- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset tacking

Module picture as below showing

2. GENERAL SPECIFICATION

General Specification	
Chip Set	RTL8761BTV
Product ID	FSC-BT836B
Dimension	13mm x 26.9mm x 2.4mm
Bluetooth Specification	Bluetooth V5.3 (Dual Mode)
Power Supply	3.3 Volt DC
Output Power	+4.5 dBm (default for all data rate) +10 dBm (BR/BLE)(Max.) +7.5 dBm (EDR)(Max.)
Sensitivity	-94 dBm(2Mbps EDR)(Min.) -98 dBm(BLE)(Min.)
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	GFSK, π/4-DQPSK, 8-DPSK
Baseband Crystal OSC	40MHz
Hopping & channels	1600hops/sec, 1MHz channel space,79 Channels(BT 5.x to 2MHz channel space)
RF Input Impedance	50 ohms
Antenna	Integrated chip antenna
Interface	Data: UART (Standard), I^2C Others: PIO, AIO, PWM.USB
Profile	SPP, HID, GATT, ATT, GAP
Advanced Feature	Airsync, iBeacon, OTA
Temperature(Optional)	0ºC to +70 ºC -20ºC to +85 ºC
Humidity	60% （Max）
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

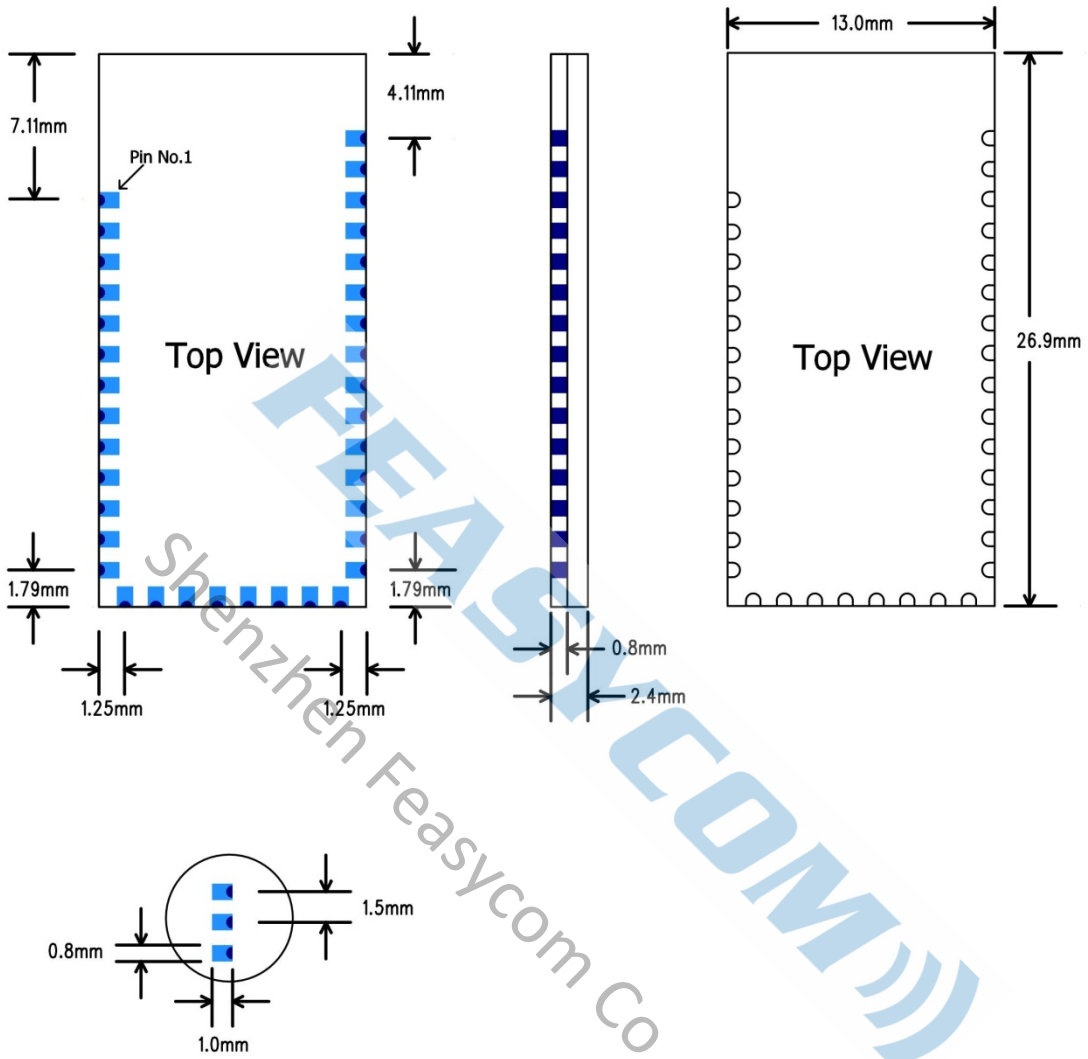

Figure 1

4. PIN DEFINITION DESCRIPTIONS

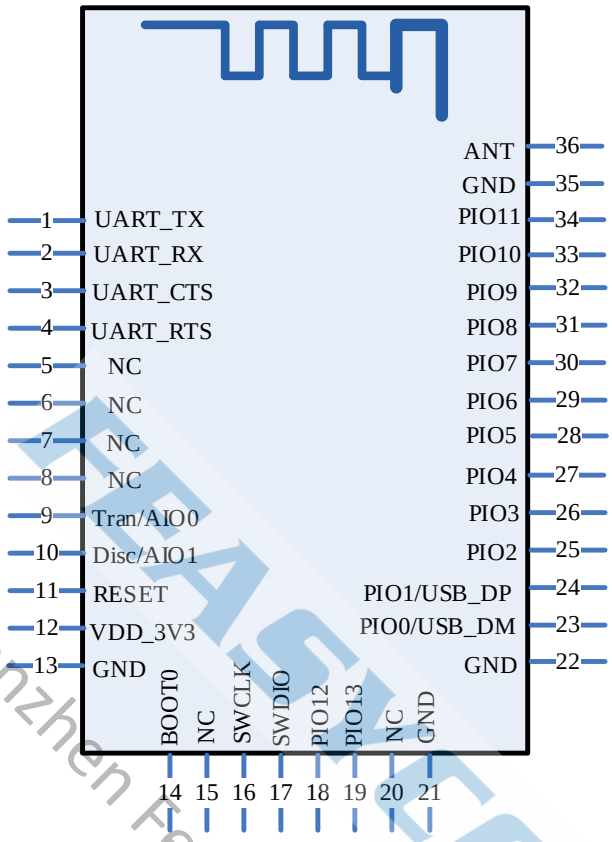

Figure 2: FSC-BT836B PIN Diagram

Pin NO.	Pin Name	Type	Pin Descriptions
1	UART_TX	CMOS output	UART data output
2	UART_RX	CMOS input	UART data input
3	UART_CTS	CMOS input	UART clear to send active low Alternative Function: Programmable input/output line
4	UART_RTS	CMOS output	UART request to send active low Alternative Function: Programmable input/output line
5	NC	NC	NC
6	NC	NC	NC
7	NC	NC	NC
8	NC	NC	NC

9	Tran/AIO0	I/O	Host MCU change UART transmission mode. (Default) Alternative Function: Analogue programmable I/O line.
10	Disc/AIO1	I/O	Host MCU disconnect bluetooth. (Default). Alternative Function: Analogue programmable I/O line.
11	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
12	VDD_3V3	VDD	Power supply voltage 3.3V
13	GND	VSS	Power Ground
14	BOOT0	CMOS input	The default is low. (internal 10K resistance drop) UART DFU Mode, Enabled at startup when set to high level, Disabled by default
15	NC	NC	*NC*
16	SWCLK	Bi-directional	Debugging through the clk line(Default)
17	SWDIO	Bi-directional	Debugging through the data line(Default)
18	PIO12	Bi-directional	Programmable input/output line ***Alternative Function: UART3 data output***
19	PIO13	Bi-directional	Programmable input/output line ***Alternative Function: UART3 data input***
20	NC	NC	*NC*
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	PIO0/USB_DM	Bi-directional	Programmable input/output line Alternative Function: ***USB_DM(optional)***
24	PIO1/USB_DP	Bi-directional	Programmable input/output line Alternative Function: ***USB_DP(optional)***
25	PIO2	Bi-directional	Programmable input/output line

26	PIO3	Bi-directional	Programmable input/output line
27	PIO4	Bi-directional	Programmable input/output line Alternative Function: BT Power Mode, low level in run mode, it will be set to high level when fall asleep.
28	PIO5	Bi-directional	Programmable input/output line
29	PIO6	Bi-directional	Programmable input/output line Alternative Function: I^2C Serial Clock input/output
30	PIO7	Bi-directional	Programmable input/output line Alternative Function:I^2C Serial Data input/output
31	PIO8	Bi-directional	Programmable input/output line
32	PIO9	Bi-directional	Programmable input/output line Alternative Function: LED(Default)
33	PIO10	Bi-directional	Programmable input/output line Alternative Function: BT Status(Default)
34	PIO11	Bi-directional	Programmable input/output line
35	GND	VSS	Power Ground
36	EXT_ANT	RF signal output	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

Table 2

5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT836B is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT836B module	Data from FSC-BT836B module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT836B module	Request to send output of FSC-BT836B module
UART-CTS	Host	Clear to send input of FSC-BT836B module

Table 3

Possible UART Settings

Property	Possible Values
BCSP-Specific Hardware	Enable or Disable
Baudrate	1200bps to 921Kbps
Flow Control	RTS/CTS or None
Data bit length	8bits
Parity	None, Odd or Even
Number of Stop Bits	1 or 2

Table 4

Default Data Format

Property	Possible Values
Baudrate	115.2Kbps
Flow Control	None
Data bit length	8bit
Parity	None

Number of Stop Bits	1

Table 5

5.2 AIO , PIO lines I²C and USB

Up to 19 programmable bidirectional input/output (I/O) can be used.
Two general purpose analogue interface pin can be used.
PIO6 and PIO7 can be used as I²C interface.

Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

Universal serial bus (USB)

The FSC-BT836B embeds a full-speed USB device peripheral compliant with the USB specification version 2.0.
The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support.

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 4 and Figure 5 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max

- Cycloe interval：5 minus

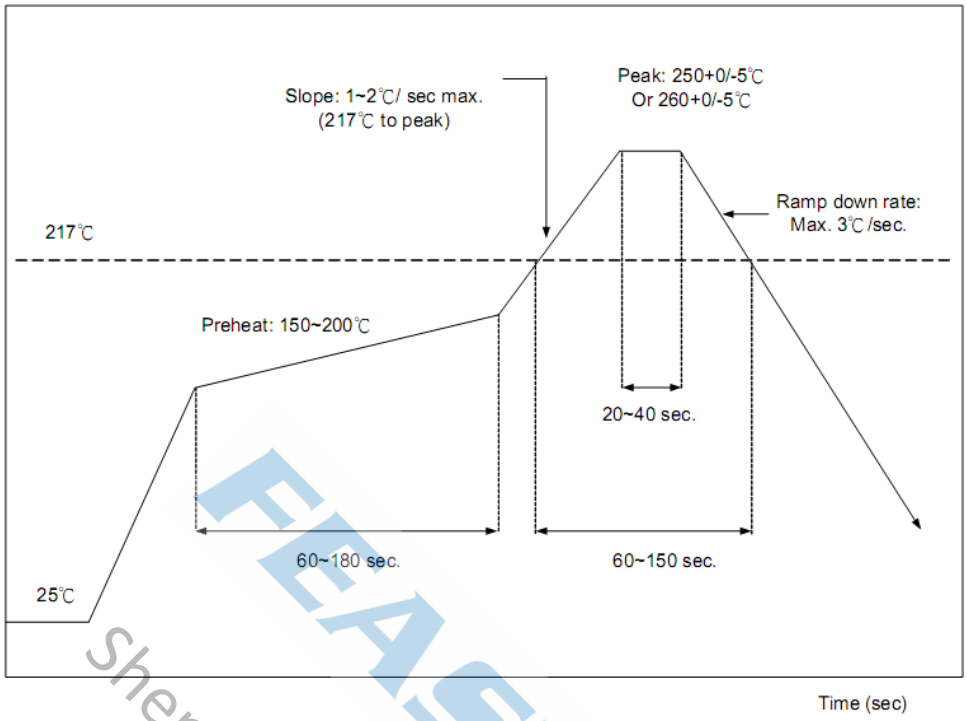

Figure 3: Typical Lead-free Re-flow Solder Profile

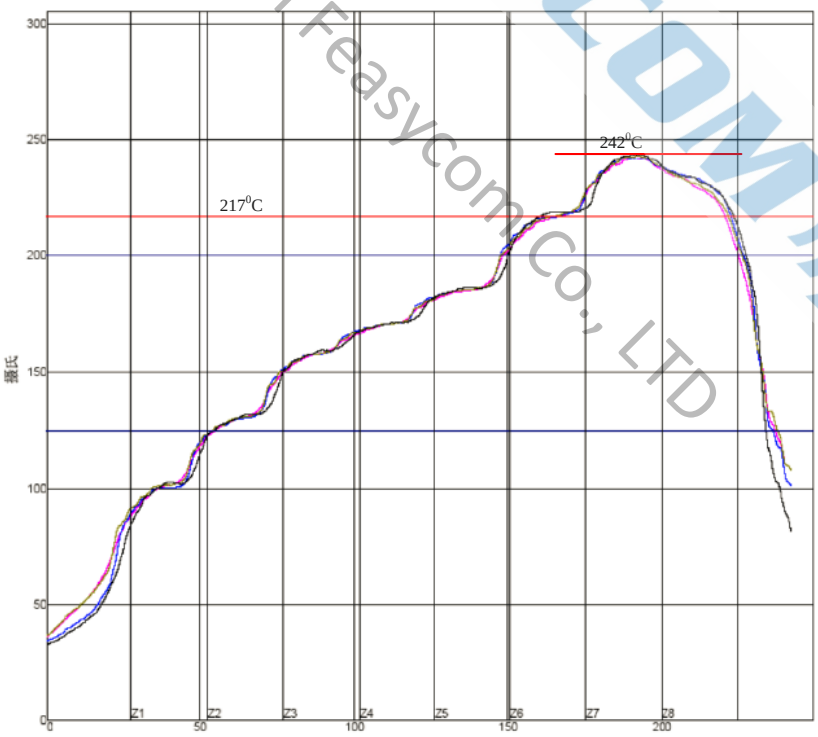

Figure 4: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT836B will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －20℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －20℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in seven days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT836B is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

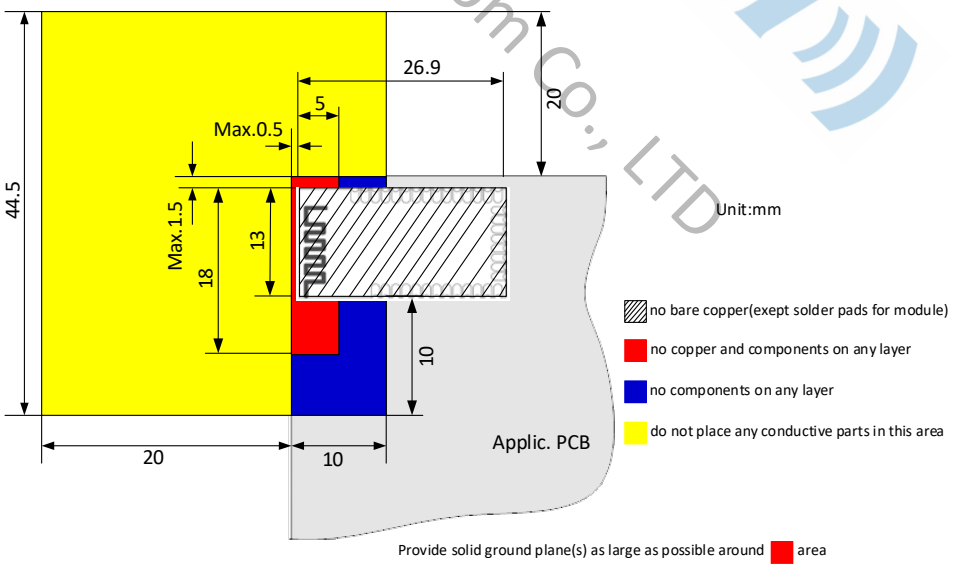

Figure 5: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9. Application Schematic