



FSC-BW104

Bluetooth 5.0 + Dual-band 2x2 802.11ac Module Datasheet

Version 1.0

Copyright © 2013-2021 Feasycom Technology. All Rights Reserved.

Feasycom Technology reserves the right to make corrections, modifications, and other changes to its products, documentation and services at anytime. Customers should obtain the newest relevant information before placing orders. To minimize customer product risks, customers should provide adequate design and operating safeguards. Without written permission from Feasycom Technology, reproduction, transfer, distribution or storage of part or all of the contents in this document in any form is prohibited.

Revision History

Version	Date	Notes	Approved By
1.0	2020/04/10	Initial Version	Devin Wan

Contact Us

Shenzhen Feasycom Technology Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District, Shenzhen, 518102, China
Tel: 86-755-27924639

Contents

1. INTRODUCTION	5
2. GENERAL SPECIFICATION	7
3. HARDWARE SPECIFICATION.....	8
3.1 BLOCK DIAGRAM AND PIN DIAGRAM.....	8
3.2 PIN DEFINITION DESCRIPTIONS.....	9
4. PHYSICAL INTERFACE	11
4.1 UART INTERFACE	11
4.2 BLUETOOTH PCM INTERFACE	12
4.3 WLAN HOST INTERFACES.....	15
4.3.1 SDIO V3.0.....	15
4.3.2 SDIO Default Mode Timing	16
4.3.3 SDIO High-Speed Mode Timing.....	17
4.3.4 SDIO Bus Timing Specifications in SDR Modes.....	18
4.3.5 Device Input Timing.....	19
4.3.6 Device Output Timing.....	19
4.3.7 SDIO Bus Timing Specifications in DDR50 Mode.....	21
5. ELECTRICAL CHARACTERISTICS	22
5.1 ABSOLUTE MAXIMUM RATINGS	22
5.2 RECOMMENDED OPERATING CONDITIONS	22
5.3 RF CHARACTERISTIC	23
5.3.1 WLAN RF Characteristics(Transmitter).....	23
5.3.2 WLAN RF Characteristics(Receive)	23
5.3.3 Bluetooth RF Characteristics.....	24
5.4 DIGITAL PAD INTERNAL PULL RESISTOR.....	24
5.5 POWER UP/DOWN SEQUENCE	25
5.6 POWER CONSUMPTION.....	26
6. MSL & ESD	26
7. RECOMMENDED TEMPERATURE REFLOW PROFILE	26
8. MECHANICAL DETAILS	28
8.1 MECHANICAL DETAILS	28
9. HARDWARE INTEGRATION SUGGESTIONS.....	29
9.1 SOLDERING RECOMMENDATIONS.....	29
9.2 LAYOUT GUIDELINES(INTERNAL ANTENNA)	30
9.3 LAYOUT GUIDELINES(EXTERNAL ANTENNA).....	30
9.3.1 Antenna Connection and Grounding Plane Design.....	31
9.4 SDIO LINES LAYOUT GUIDELINE	32
9.5 HCI LINES LAYOUT GUIDELINE	32
9.6 PCM LINES LAYOUT GUIDELINE	32



9.7	RTC Clock(32.768kHz) LINES LAYOUT GUIDELINE	33
9.8	POWER TRACE LINES LAYOUT GUIDELINE.....	33
9.9	GROUND LINES LAYOUT GUIDELINE.....	33
10.	PRODUCT PACKAGING INFORMATION	33
10.1	DEFAULT PACKING.....	33
10.2	PACKING BOX(OPTIONAL).....	34
11.	APPLICATION SCHEMATIC.....	35

1. INTRODUCTION

Overview

FSC-BW104 uses the gauge level IC QCA6574A, it is a single-die wireless local area network (WLAN) and Bluetooth (BT) combo solution to support 2x2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards and BT 5.0 enabling seamless integration of WLAN/BT and Low Energy technology.

FSC-BW104 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. As a result, enhanced overall quality for simultaneous voice, video, and transmission is achieved.

FSC-BW104 is an appropriate product for designers who want to add wireless capability to their products. Let all of the system high design flexibility, short development cycle, and quick time-to-market.

General Features

- Highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 5 GHz 802.11ac, or 2.4/5GHz 802.11n WLAN applications
- Supports BT 5.0, ANT+ and is backward-compatible with previous BT versions from v1.2
- Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Rx Space Time Block Code (STBC)
- Supports 20/40 MHz at 2.4 GHz and supports 20/40/80MHz at 5 GHz
- Supports BT-WLAN coexistence and ISM-LTE coexistence
- Support BT for class 1 and class 2 power-level transmissions without requiring an external PA

(power amplifier)

- Enhanced qualification based on selective AEC Q100 and JEDEC test cases
- Single-stream spatial multiplexing up to 433.3 Mbps data rate. (Under dual-antenna status, 802.11ac:Up to 867Mbps)
- Low power SDIO3.0/SDIO2.0 interface for WLAN and UART/PCM interface for BT
- UART(Max Baud Rate 3.2Mbps)
- Stamp module suitable for Surface Mounted Technology (SMT)
- Iron Shielding case
- Stamp-53 package
- Dimension(Iron Shielding Case) : 23.4mm(L) x 19.4mm(W) x 2.6mm(H)
- Operating Voltage :
VBAT : 3.14 to 3.46V ; VIO: 1.71 to 3.46V
- RoHS / REACH Compliant
- External Antenna
- Support GATT,HID,DUN,FTP,ANCS
- Support HFP, A2DP, AVRCP, PBAP, SPP
- Support Android /Linux

Application

- Car audio and video system
- Measurement systems
- STB/OTT/IPTV

Module picture as below showing



Figure 1: FSC-BW104 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.0+EDR
Frequency Band		2402MHz~2480MHz
Bluetooth class		Class 1 , Class 2
Range, line of sight		Up to 10m
Transmit power		9dBm Max
Receiver sensitivity		-89dBm
Support mode		Slave and Master
Profiles		HFP, A2DP, AVRCP, SPP, PBAP, HID, DUN, FTP, GATT, ANCS
Maximum throughput		3Mbps
Interface		UART/PCM
WIFI		
Wi-Fi feature		2.4G: IEEE802.11 b/g/n radio 5G: IEEE802.11 a/n/ac radio
Range, line of sight		Up to 100m
Frequency Band		2.4GHz and 5GHz frequency band
Transmit power		17dBm(Maximum) 10dBm(Minimum)
Receiver sensitivity		-80dBm@11Mbps -71dBm@54Mbps -70dBm@HT20 MCS7 -70dBm@HT40 MCS7 -60dBm@VHT80 MCS9
Profiles		WIFI-AP(access point), WIFI-Station
Maximum throughput		802.11b:Up to 11Mbps 802.11g:Up to 54Mbps 802.11n:Up to 300Mbps 802.11ac:Up to 867Mbps(Under dual-antenna status)
Security		WEP, TKIP, AES, WPA, WPA2
Interface		SDIO
General		
Size		23.4mm(L) x 19.4mm(W) x 2.6mm(H)
Hardware Interface		UART, GPIO, SDIO, PCM/I2S
Antenna		External (Dual-band antenna, supporting 2.4GHz and 5.8GHz frequencies)
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Operating voltage (VBAT)		3.3V (Typ.)

VIO	1.8V~3.3V(Typ.)	
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity	10% ~ 90% non-condensing	
MSL grade:	MSL 3	
ESD grade:	Human Body Model: Pass ± 2000 V, all pins	
	Charge device model: Pass ± 250 V, all pins	

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

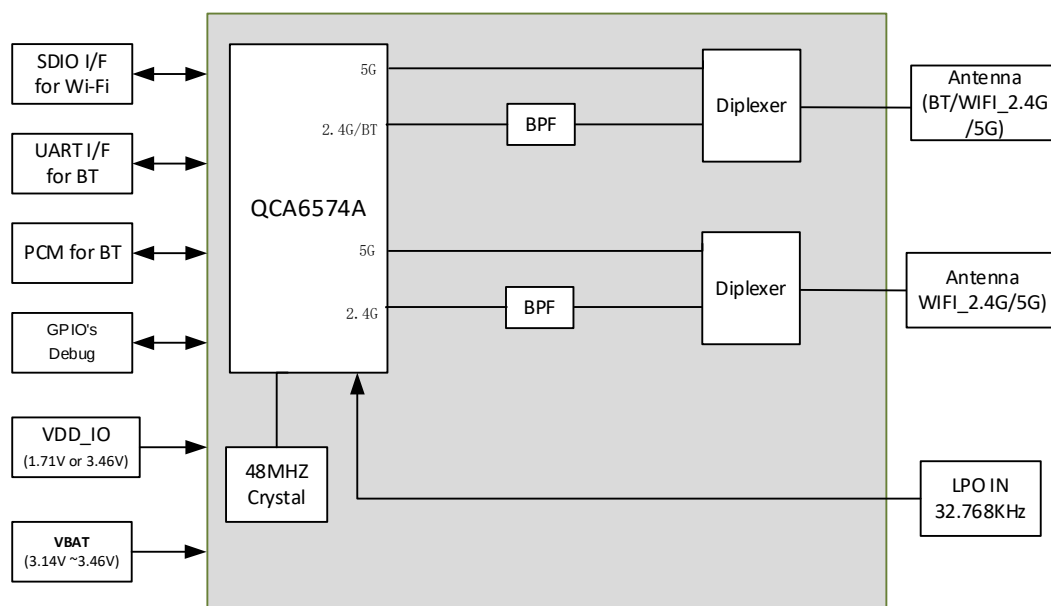


Figure 2: Block Diagram

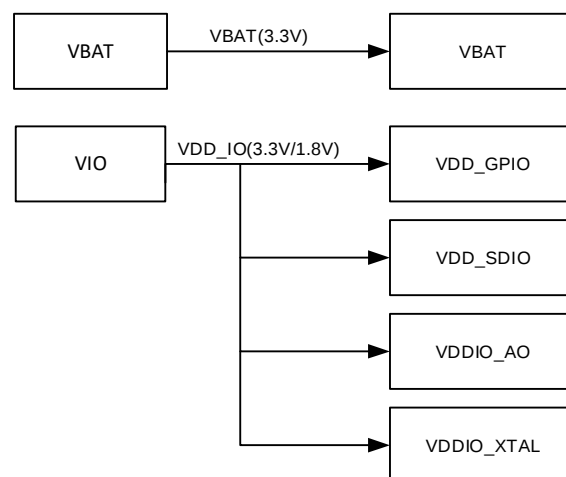


Figure 3: Block diagram of the power section

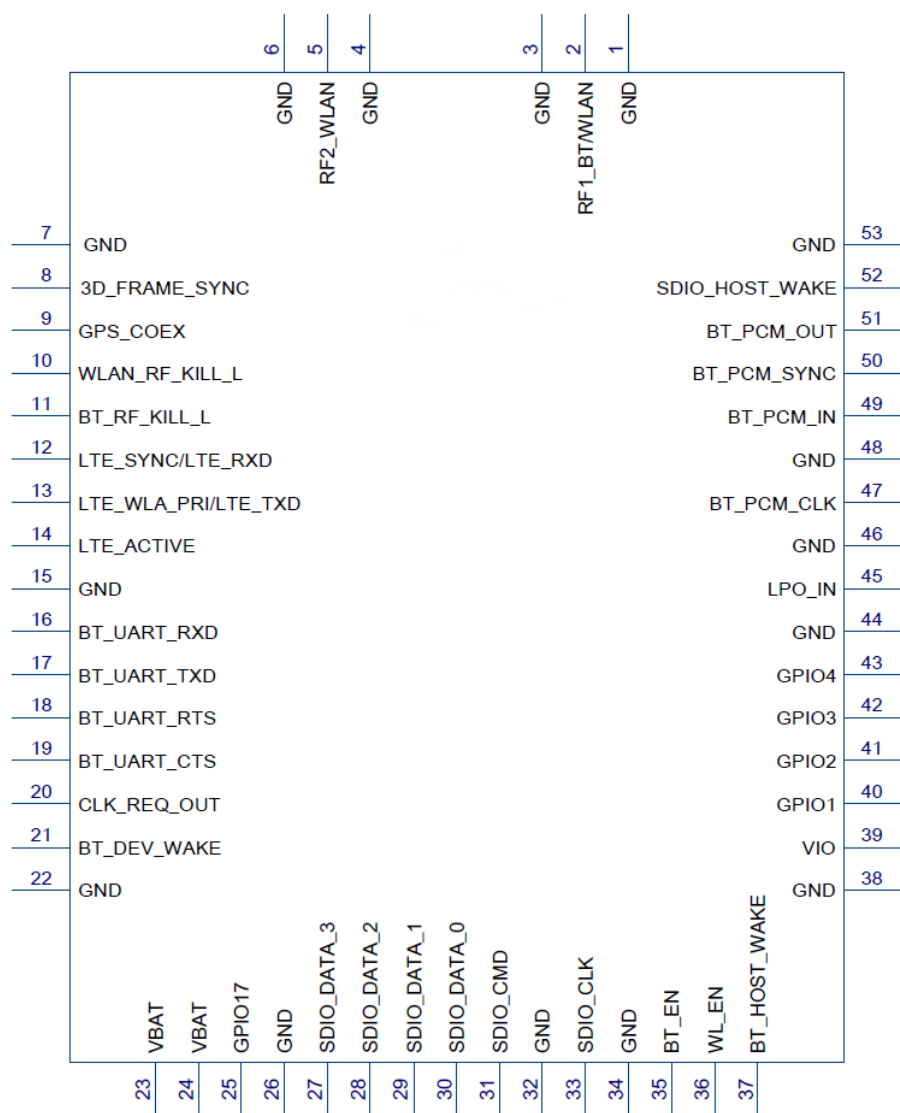


Figure 4: FSC-BW104 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND		Ground	
2	RF1_BT/WLAN	RF	WLAN 2.4/5GHz and Bluetooth RF input/output port	
3	GND		Ground	
4	GND		Ground	
5	RF2_WLAN	RF	WLAN 2.4/5GHz RF input/output port	
6	GND		Ground	
7	GND		Ground	
8	3D_FRAME_SYNC	I/O	Frame sync signal from TV to sync with 3D glass via Bluetooth. NC if not used.	

9	GPS_COEX	I/O	GPS co-existence signal. High means WLAN is in transmit. NC if not used.
10	WLAN_RF_KILL_L	I	Turn-off WLAN RF analog and front-end. Active low. NC if not used.
11	BT_RF_KILL_L	I	Turn-off Bluetooth RF analog and front-end. Active low. NC if not used.
12	LTE_SYNC/LTE_RXD	I/O	LTE co-existence signal. LTE_UART_RXD or LTE_FS. NC if not used.
13	LTE_WLA_PRI/LTE_TXD	I/O	LTE co-existence signal. LTE_UART_TXD or LTE_PRI. NC if not used.
14	LTE_ACTIVE	I/O	LTE co-existence signal (it is not required if using 2-wire interface for LTE co-existence. NC if not used.
15	GND		Ground
16	BT_UART_RXD	I	BT UART I/F
17	BT_UART_TXD	O	BT UART I/F
18	BT_UART_RTS	I/O	BT UART I/F
19	BT_UART_CTS	I/O	BT UART I/F
20	CLK_REQ_OUT	O	Clock request output. NC if not used
21	BT_DEV_WAKE	I	Bluetooth wake-up from host; active high. NC if not used.
22	GND		Ground
23	VBAT	PWR	3.3V Supply Voltage
24	VBAT	PWR	3.3V Supply Voltage
25	GPIO17	I/O	GPIO
26	GND		Ground
27	SDIO_DATA_3	I/O	SDIO data bus D3
28	SDIO_DATA_2	I/O	SDIO data bus D2
29	SDIO_DATA_1	I/O	SDIO data bus D1
30	SDIO_DATA_0	I/O	SDIO data bus D0
31	SDIO_CMD	I	SDIO command signal
32	GND		Ground
33	SDIO_CLK	I	SDIO clock signal
34	GND		Ground
35	BT_EN	I	Bluetooth Function Enable(High Active)(BT_Reset)
36	WL_EN	I	Wi-Fi Function Enable(High Active) (Wi-Fi_Reset)
37	BT_HOST_WAKE	O	Wake-up the host from BT; active high. NC if not used.
38	GND		Ground
39	VIO	PWR	Voltage supply for all IO signals. 1.8V or 3.3V
40	GPIO1	I/O	GPIO
41	GPIO2	I/O	GPIO
42	GPIO3	I/O	GPIO
43	GPIO4	I/O	GPIO
44	GND		Ground
45	LPO_IN	I	External low-power 32.768 kHz clock input.
46	GND		Ground

47	BT_PCM_CLK	I/O	BT PCM/I2S Clock; NC if not used.
48	GND		Ground
49	BT_PCM_IN	I	BT PCM/I2S Bus. Data in ; NC if not used.
50	BT_PCM_SYNC	I/O	BT PCM/I2S Bus. Frame sync ; NC if not used.
51	BT_PCM_OUT	O	BT PCM/I2S Bus. Data out ; NC if not used
52	SDIO_HOST_WAKE	O	Wi-Fi Interrupt Request
53	GND		Ground

PWR= Power Input; I/O=Bi-directional; I=Input; O=Output; RF=RF Pin; GND=Ground; F=Floating (Not Connected)

4. PHYSICAL INTERFACE

4.1 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 3.2 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbps.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

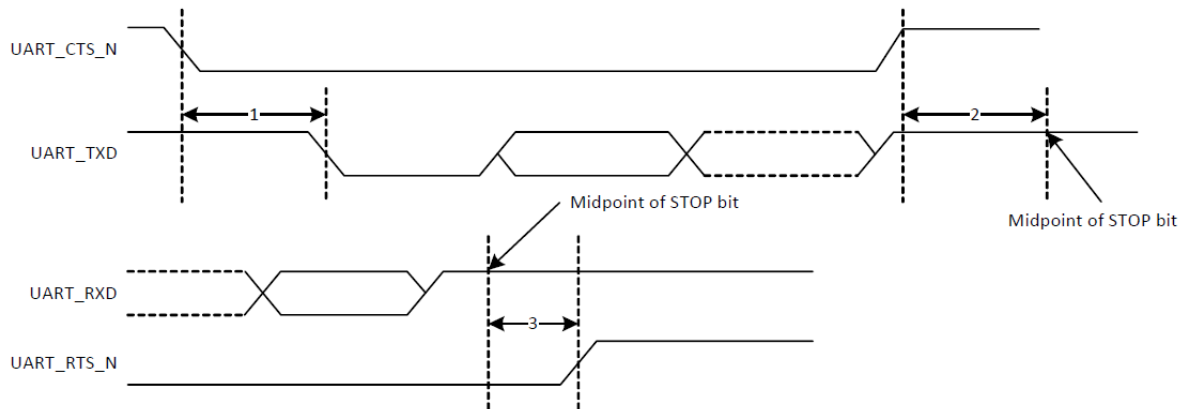
FSC-BW104 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

FSC-BW104 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Table 3: Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 9600 baud ($\leq 0\%$ Error)
	Standard 115200bps ($\leq 1.6\%$ Error)
	Maximum 3.2Mbps ($\leq 0\%$ Error)
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

**Figure 5:** UART Timing**Table 4:** UART Timing Specifications

Parameter	Min	Type	Max	Unit
Delay time, UART_CTS_N low to UART_TXD valid			1.5	Bit period
Setup time, UART_CTS_N high before midpoint of stop bit			0.5	Bit period
Delay time, midpoint of stop bit to UART_RTS_N high			0.5	Bit period

4.2 Bluetooth PCM Interface

The pulse coded modulation (PCM) interface connects the FSC-BW104 to the phone's audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDD_IO supply. Their I/O performance specifications meet the requirements stated.

FSC-BW104 PCM interface has been designed to minimize audio latency. The typical audio latencies for various packet types as follows.

Table 5: Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 Tesco=6, Wesco=0	4.4mS
EV3 Tesco=6, Wesco=2	5.7mS

EV3 Tesco=6,Wesco=4

6.9mS

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether FSC-BW104 PCM interface is configured as master or slave:

- When FSC-BW104 PCM interface is the master : PCM_CLK and PCM_SYNC are outputs from the device to the PCM bus slave(s).
- When FSC-BW104 PCM interface is the slave : PCM_CLK and PCM_SYNC are inputs to the device from the PCM bus master.

Table 6: PCM interface specifications

Parameter	Min	Type	Max	Unit
Clock rate(Slave)—Determined by the master	64	-	2048	KHz
Clock rate(Master)—(32MHz *N/4000),in which N is an integer	64	-	2048	KHz
Frame size	1	8	256	Bits
Slot size	1	13	16	Bits
Slot number—Number of slots that can be configured per frame	1	-	32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following tables and illustrations.

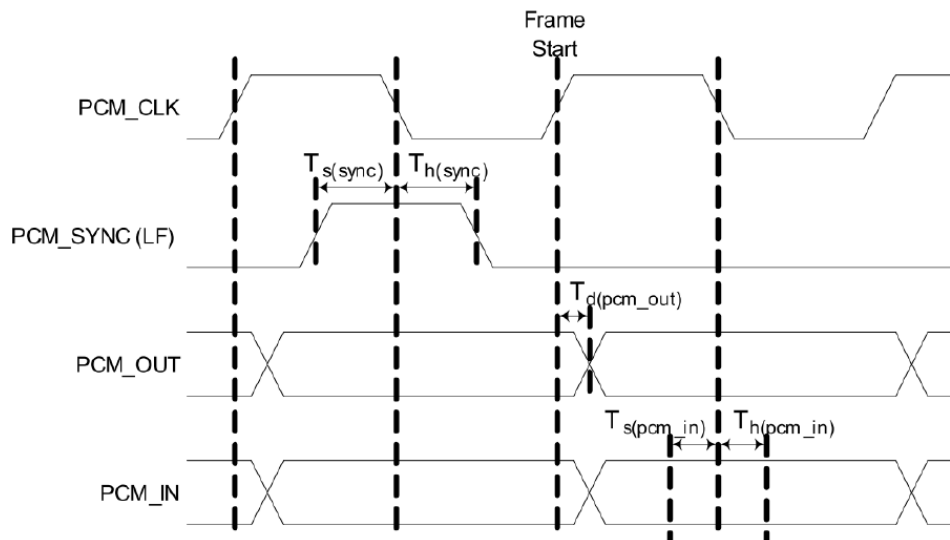
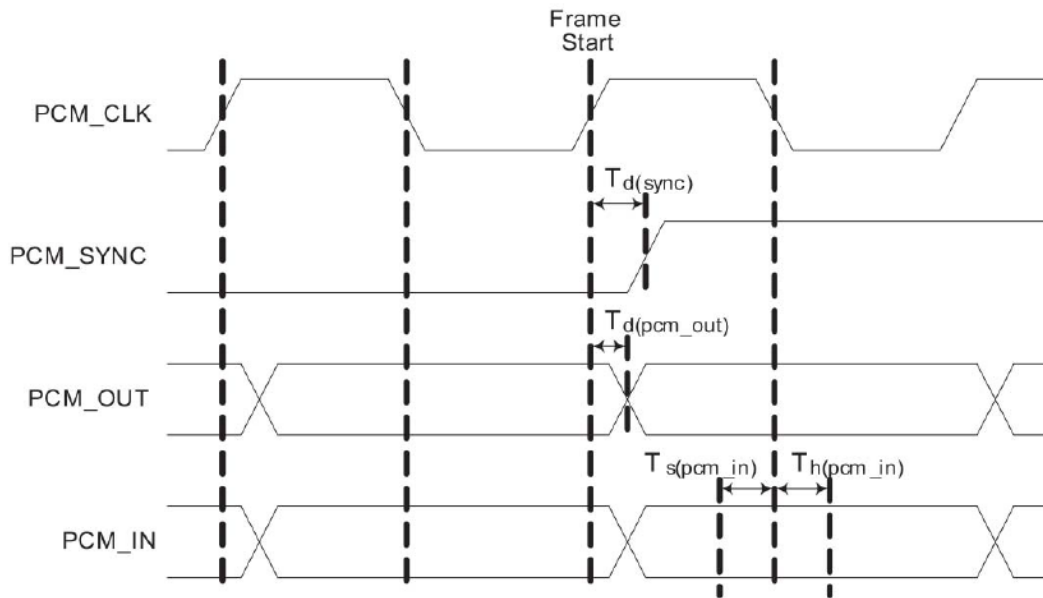
**Figure 6:** PCM interface timing diagram(slave)

Table 7: PCM interface timing in slave mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Setup time PCM_SYNC to PCM_CLK fall	0	-	-	ns
Hold time PCM_CLK fall to PCM_SYNC fall	150	-	-	ns
Delay from PCM_CLK rise to PCM_OUT	0	-	150	ns
Setup time PCM_IN to PCM_CLK fall	0	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

**Figure 7:** PCM interface timing diagram(master)**Table 8:** PCM interface timing in master mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Delay from PCM_CLK rise to long SYNC	-10	-	50	ns
Delay from PCM_CLK rise to PCM_OUT	-10	-	50	ns
Setup time PCM_IN to PCM_CLK fall	50	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

4.3 WLAN Host Interfaces

4.3.1 SDIO V3.0

The module WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208 MHz (1.8V signaling).
- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The QCA6574A is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

SDIO mode is enabled by strapping options. Refer to next Table WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient

Table 9: SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data line 0
DATA1	Data line 1 or Interrupt
DATA2	Data line 2 or Read Wait
DATA3	Data line 3
CLK	Clock
CMD	Command line

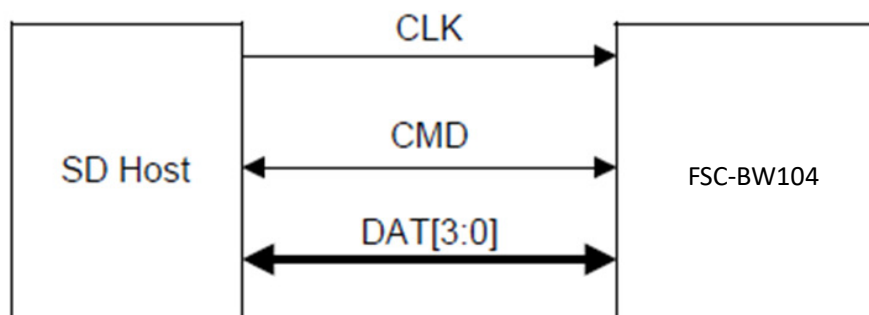


Figure 8: Signal Connections to SDIO Host (SD 4-Bit Mode)

4.3.2 SDIO Default Mode Timing

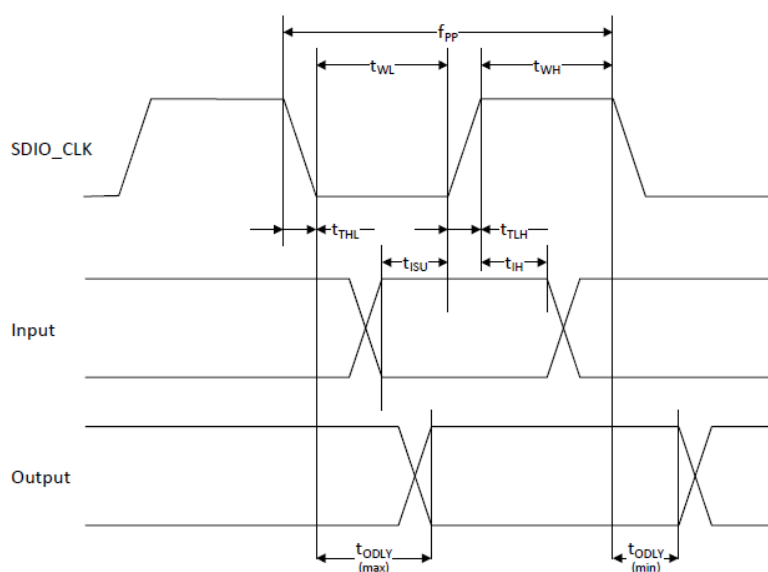


Figure 9: SDIO Bus Timing (Default Mode)

Table 10: SDIO Bus Timing^a Parameters (Default Mode)

Parameter	Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)				
Frequency – Data Transfer mode	0	-	25	MHz
Frequency – Identification mode	0	-	400	KHz
Clock low time	10	-	-	ns
Clock high time	10	-	-	ns
Clock rise time	8	-	10	ns
Clock fall time	0	-	10	ns
Inputs: CMD, DAT (referenced to CLK)				

Input setup time	5	-	-	ns
Input hold time	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)				
Output delay time - Data Transfer mode	0	-	14	ns
Output delay time - Identification mode	0	-	50	ns

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. Min. $(V_{ih}) = 0.7 \times VDDIO$ and max $(V_{il}) = 0.2 \times VDDIO$.

4.3.3 SDIO High-Speed Mode Timing

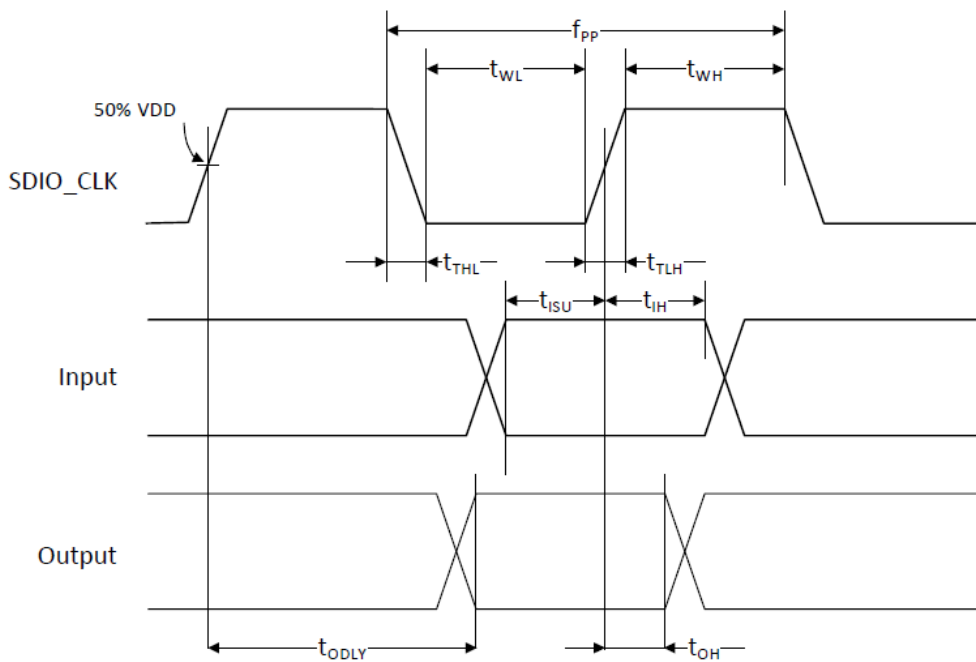


Figure 10: SDIO Bus Timing (Default Mode)

Table 11: SDIO Bus Timing^a Parameters (High-Speed Mode)

Parameter	Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)				
Frequency - Data Transfer mode	0	-	50	MHz
Frequency - Identification mode	0	-	400	KHz
Clock low time	7	-	-	ns
Clock high time	7	-	-	ns
Clock rise time	-	-	3	ns
Clock fall time	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)				

Input setup time	6	-	-	ns
Input hold time	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)				
Output delay time – Data Transfer mode	-	-	14	ns
Output hold time	2.5	-	-	ns
Total system capacitance (each line)	-	-	40	

a. Timing is based on $CL \leq 40\text{pF}$ load on CMD and Data.

b. Min. (V_{ih}) = $0.7 \times V_{DDIO}$ and max (V_{il}) = $0.2 \times V_{DDIO}$.

4.3.4 SDIO Bus Timing Specifications in SDR Modes

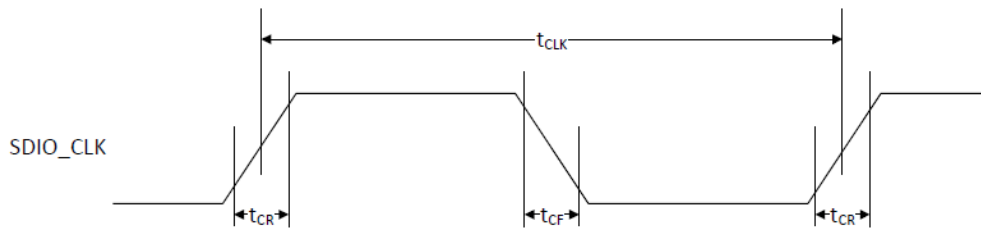


Figure 11: SDIO Clock Timing (SDR Modes)

Table 12: SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Min	Type	Max	Unit	Remark
	40	-	-	ns	SDR12 mode
	20	-	-	ns	SDR25 mode
	10	-	-	ns	SDR50 mode
	4.8	-	-	ns	SDR104 mode
	-	-	3	ns	$t_{CR}, t_{CF} < 2.00 \text{ ns (max.) @100 MHz, CCARD} = 10 \text{ pF}$ $t_{CR}, t_{CF} < 0.96 \text{ ns (max.) @208 MHz, CCARD} = 10 \text{ pF}$
Clock duty cycle	30	-	70	%	ns

4.3.5 Device Input Timing

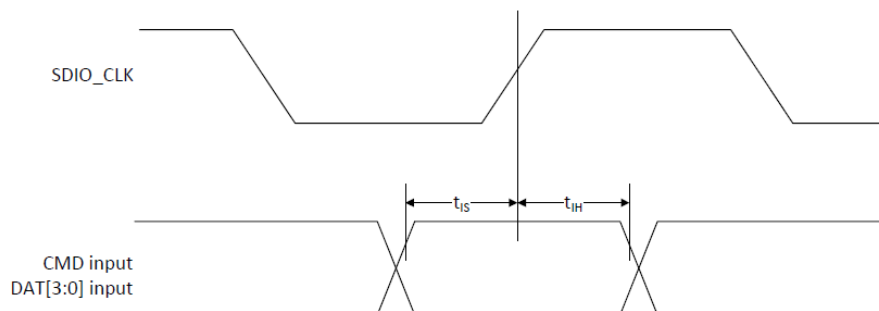


Figure 12: SDIO Bus Input Timing (SDR Modes)

Table 13: SDIO Bus Input Timing Parameters (SDR Modes)

symbol	Min	Type	Max	Unit	Remark
SDR104 Mode					
t_{IS}	1.4	-	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.8	-	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$
SDR50 Mode					
t_{IS}	3.0	-	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.8	-	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$
SDR25 Mode					
t_{IS}	3.0	-	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.8	-	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$
SDR12 Mode					
t_{IS}	3.0	-	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.8	-	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$

4.3.6 Device Output Timing

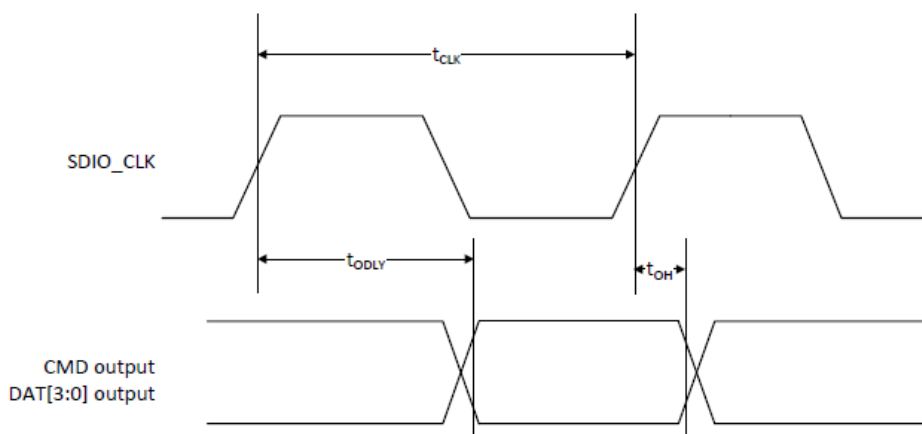
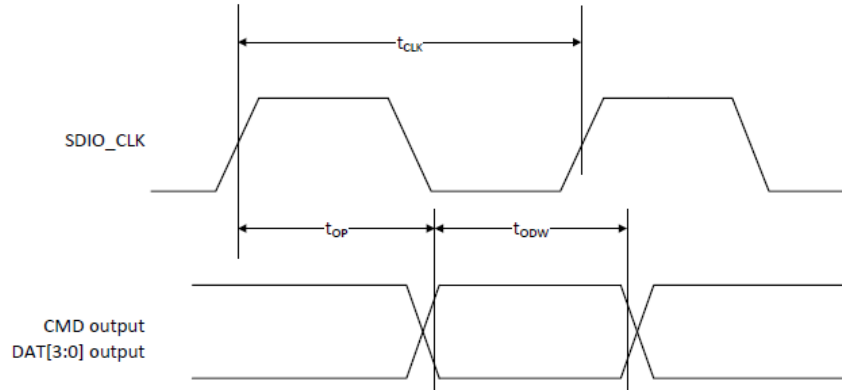


Figure 13: SDIO Bus Output Timing (SDR Modes up to 100MHz)

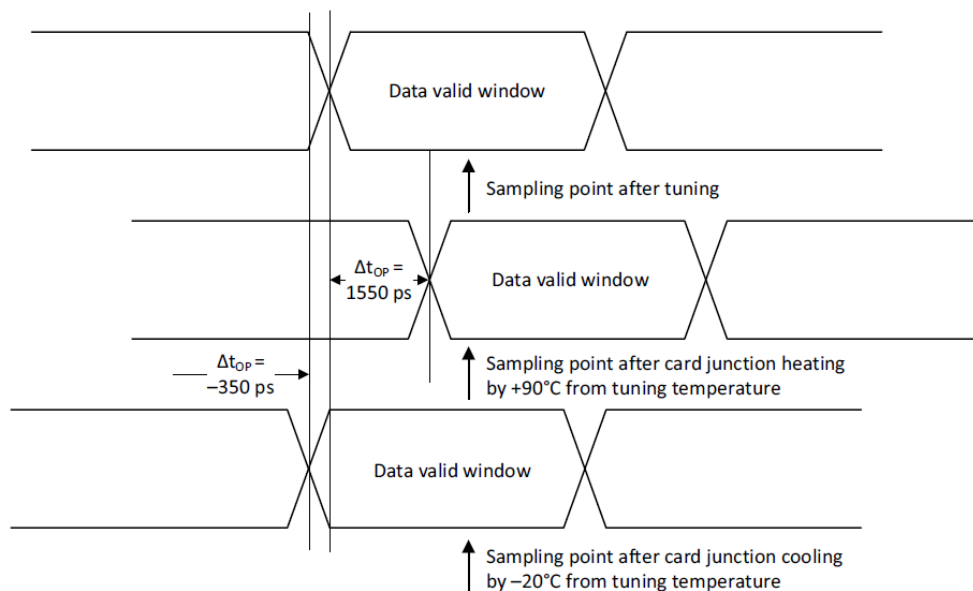
Table 14: SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

symbol	Min	Type	Max	Unit	Remark
t_{ODLY}	–	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
T_{OH}	1.5	–	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

**Figure 14:** SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)**Table 15:** SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

symbol	Min	Type	Max	Unit	Remark
t_{OP}	0	–	2	UI	Card output phase
Δt_{OP}	-350	–	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	–	UI	$t_{ODW} = 2.88$ ns @208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

**Figure 15:** Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

4.3.7 SDIO Bus Timing Specifications in DDR50 Mode

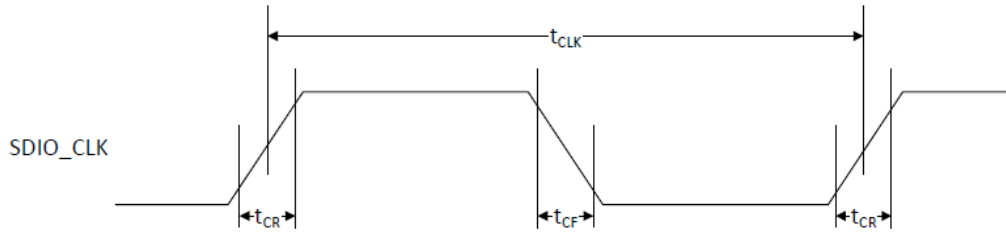


Figure 16: SDIO Clock Timing (DDR50 Mode)

Table 16: SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Remark
t_{CLK}	20	-	7.5	ns	DDR50 mode
t_{CR}, t_{CE}	-	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty cycle	45	-	55	%	-

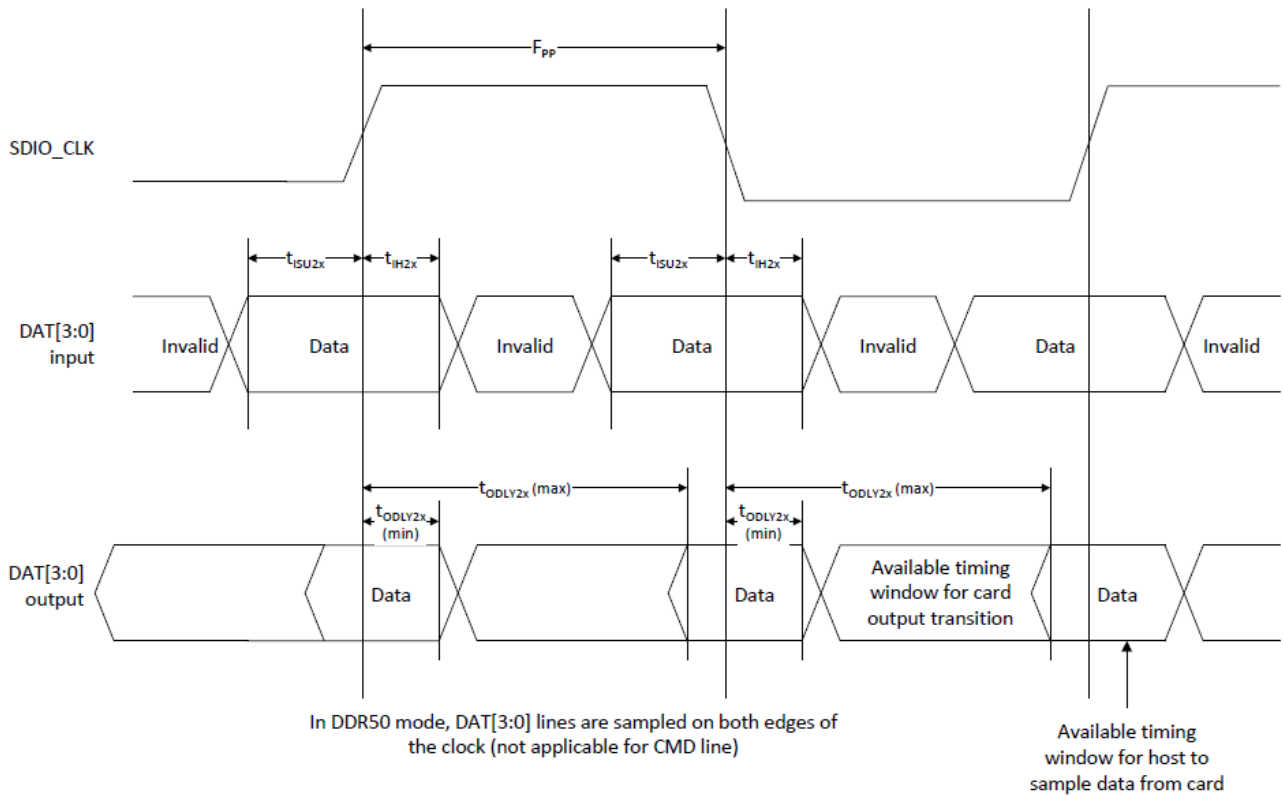


Figure 17: SDIO Data Timing (DDR50 Mode)

Table 17: SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Remark
Input CMD					
Input setup time	6	-	-	ns	C _{CARD} < 10pF (1 Card)
Input hold time	0.8	-	-	ns	C _{CARD} < 10pF (1 Card)
Outputs CMD					
Output delay time	-	-	13.7	ns	C _{CARD} < 30pF (1 Card)
Output hold time	1.5	-	-	ns	C _{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	3	-	-	ns	C _{CARD} < 10pF (1 Card)
Input hold time	0.8	-	-	ns	C _{CARD} < 10pF (1 Card)
Outputs DAT					
Output delay time	-	-	7.0	ns	C _{CARD} < 25pF (1 Card)
Output hold time	1.5	-	-	ns	C _{CARD} < 15pF (1 Card)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)

Table 18: Absolute Maximum Rating

Parameter	Min	Max	Unit
VBAT(SWREG Supply Input)	-0.3	+3.6	V
VIO(DC supply voltage for digital I/O)	-0.3	+3.6	V
Operating temperature (T _A)	-40	+85	°C
Storage temperature (T _{stg})	-40	+85	°C
Maximum junction temperature(T _j)		+105	°C
RF _{IN} Maximum RF input (reference to 50Ω input)		0	dBm

5.2 Recommended Operating Conditions

Table 19: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VBAT	3.14	3.3	3.46	V
VIO	1.71	1.8~3.3	3.46	°C
Operating temperature (T _A)	-40	25	+85	°C
Storage temperature (T _{stg})	-40	25	+85	°C

High-level input voltage	0.7 X VIO	VDD_IO + 0.3	V
Low-level input voltage	-0.3	0.3 X VIO	V
Input low leakage current	-5.0	5.0	uA
High-level output voltage	0.9 X VIO	VIO	V
Low-level output voltage	0	0.1 X VIO	V
High-level output current	3		mA
Low-level output current		-11	mA
Input capacitance		3	pF

5.3 RF Characteristic

5.3.1 WLAN RF Characteristics(Transmitter)

Table 20: WLAN Transmitter

Characteristics	Condition	EVM	Min	Type	Max	Unit
2.4GHz						
Output Power	11M CCK		13	17	18	dBm
	6M OFDM		14	16	17	dBm
	54M OFDM	-25	11	15	16	dBm
	6.5M,MCS0(HT20)		12	15	17	dBm
	65M,MCS7(HT20)	-27	10	13	15	dBm
	6.5M,MCS0(HT40)		11	14	16	dBm
	65M,MCS7(HT40)	-27	10	13	15	dBm
	180M,MCS9(VHT40)	-32	8	10	13	dBm
5GHz						
Output Power	54M OFDM	-25	10	14	16	dBm
	65M,MCS7(HT20)	-27	8	13	16	dBm
	65M,MCS7(HT20)	-27	8	13	16	dBm
	78M,MCS8(VHT20)	-30	8	13	16	dBm
	180M,MCS9(VHT40)	-32	8	11	16	dBm
	390M,MCS9(VHT80)	-32	6	10	12	dBm

5.3.2 WLAN RF Characteristics(Receive)

Table 21: WLAN Receive

Characteristics	Condition	Min	Type	Max	Unit
2.4GHz					
Sensitivity	11M CCK		-79	-80	dBm
	54M OFDM		-71	-72	dBm
	65M,MCS7(HT20)		-70	-71	dBm
5GHz					
Sensitivity	54M OFDM		-71	-74	dBm

65M,MCS7(HT20)	-70	-72	dBm
130M,MCS7(HT40)	-69	-71	dBm
78M,MCS8(VHT20)	-59	-62	dBm
180M,MCS9(VHT40)	-57	-61	dBm
390M,MCS9(VHT80)	-56	-59	dBm

5.3.3 Bluetooth RF Characteristics

Table 22: Bluetooth RF Characteristics

Characteristics	Condition	Min	Type	Max	Unit
Bluetooth specification	Version 5.0				
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)				
BT Transmitter, GFSK					
RF output power			8.5	9	dBm
Power control step		2	4	8	dB
BT Receiver Characteristics, Basic rate receiver					
Sensitivity	GFSK, BER = 0.1%		-88		dBm
	Pi/4-DQPSK, BER = 0.01%		-89		dBm
	8DPSK, BER = 0.01%		-82		
Max. useable input power	GFSK, BER = 0.1%	-5			dBm
	Pi/4-DQPSK, BER = 0.1%	-10			dBm
	8DPSK, BER = 0.1%	-10			dBm
BLE RF Characteristics					
BLE Transmitter output power			4		dBm
BT Receiver Characteristics, Low energy receiver	BER ≤ 0.1%		-88	-90	dBm

5.4 Digital pad internal pull resistor

Table 23: Digital pad internal pull resistor

Internal Pull Resistor	VIO = 1.8V		VIO = 3.3V	
	R(KΩ)		R(KΩ)	
	Min	MAX	Min	MAX
Pull down	23	72	24	60
Pull up	70	168	49	95

5.5 Power Up/Down Sequence

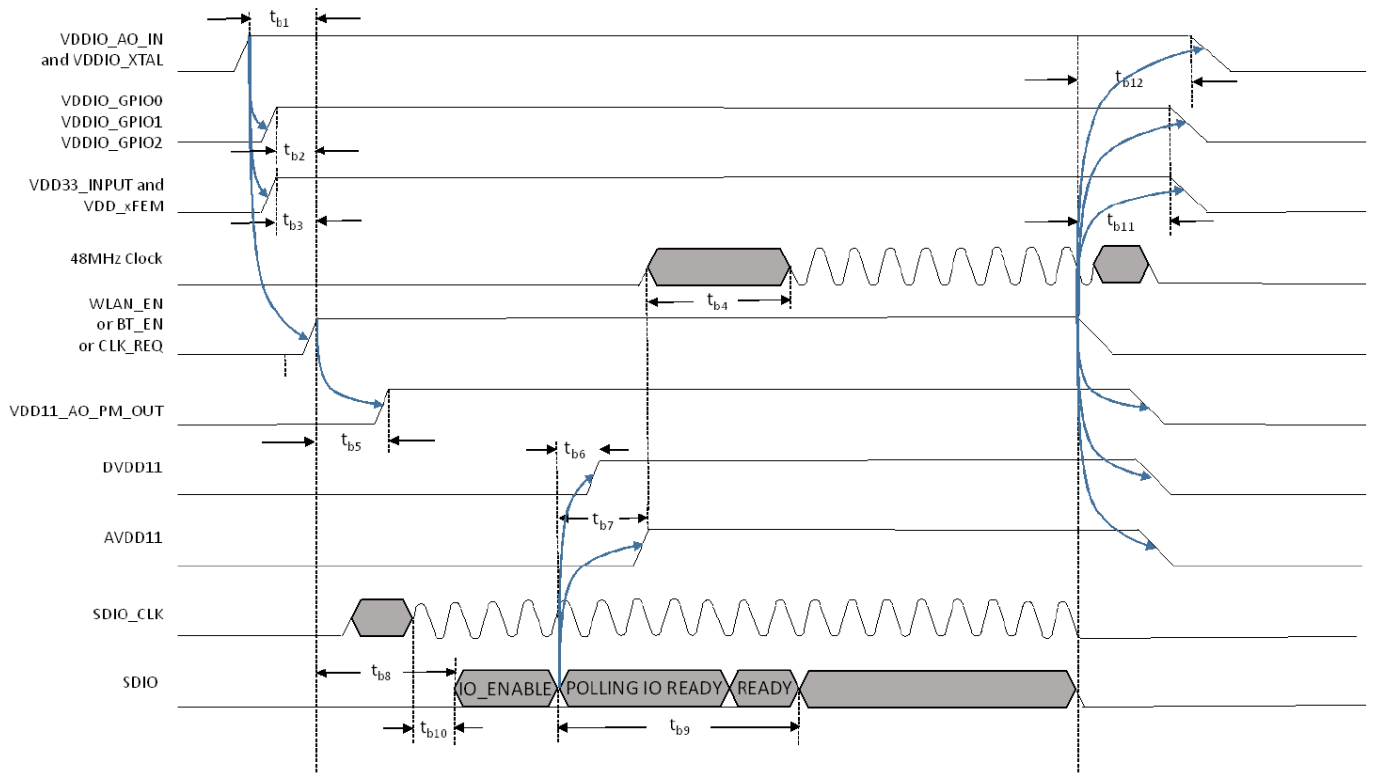


Figure 18: Power on and power off timing Sequence

Table 24: Power on and power off timing Sequence

Parameter	Min	Type	Max	Unit
tb1--VDDIO_AO valid to WL_EN input active (see note)	12			uS
tb2--VDDIO_XXX valid to WL_EN input active	10			uS
tb3--VDD33 valid to WL_EN input active	10			uS
tb4--48 MHz clock stabilization time	1			mS
tb5--WL_EN valid to AO 1.1 V established			500	uS
tb6--SDIO IO enable valid to DVDD11 established			2.5	mS
tb7--SDIO IO enable valid to AVDD11 established			3	mS
tb8--WL_EN valid to SDIO IO enable set by HOST	1			mS
tb9--SDIO IO enable valid to SDIO ready (including FW running time)			10	mS
tb10--SDIO CLK stable before SDIO IO enable set by HOST	400			uS
tb11--WL_EN de-assert to VDDIO_XXX and VDD33 ramping down	10			uS
tb12--WL_EN de-assert to VDDIO_AO ramping down (see note)	12			uS

NOTE VDDIO_AO needs to be on at first and off at last, VDDIO_AO must be > 1.62 V at all times when VDD33 > 1 V.

5.6 Power Consumption

Table 25: Power Consumption:

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VBAT	3.3V	500
VIO	3.3V	300
Testing Condition: 2.4GHz Tx MCS0 6.5Mbps		

FSC-BW104 Module Power Consumption:

500mA @ VBAT(Maximum) and 300mA @ VIO(Maximum)

Suggest customer design power capacity are 1000mA@VBAT and 500mA @ VIO for FSC-BW104 Module.

6. MSL & ESD

Table 26: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ± 2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ± 250 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccant (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccant and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意):

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

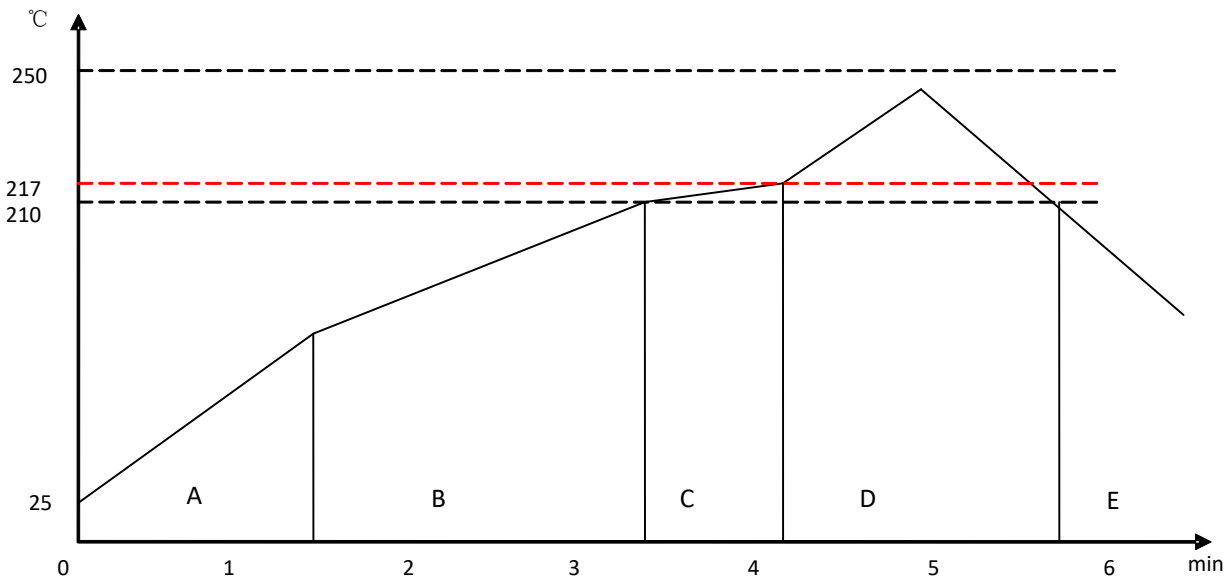
使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整。

Table 27: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit
	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

**Figure 19:** Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (T_p) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. Typical cooling rate should be 4 °C.

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 23.4mm(L) x 19.4mm(W) x 2.6mm(H) Tolerance: $\pm 0.1\text{mm}$
- Module size: 23.4mm x 19.4mm Tolerance: $\pm 0.25\text{mm}$
- Pad size: 2mmX0.8mm Tolerance: $\pm 0.1\text{mm}$
- Pad pitch: 1) 1.4mm $\pm 0.1\text{mm}$ 2) 1.2mm $\pm 0.1\text{mm}$ 3) 1.1mm $\pm 0.1\text{mm}$

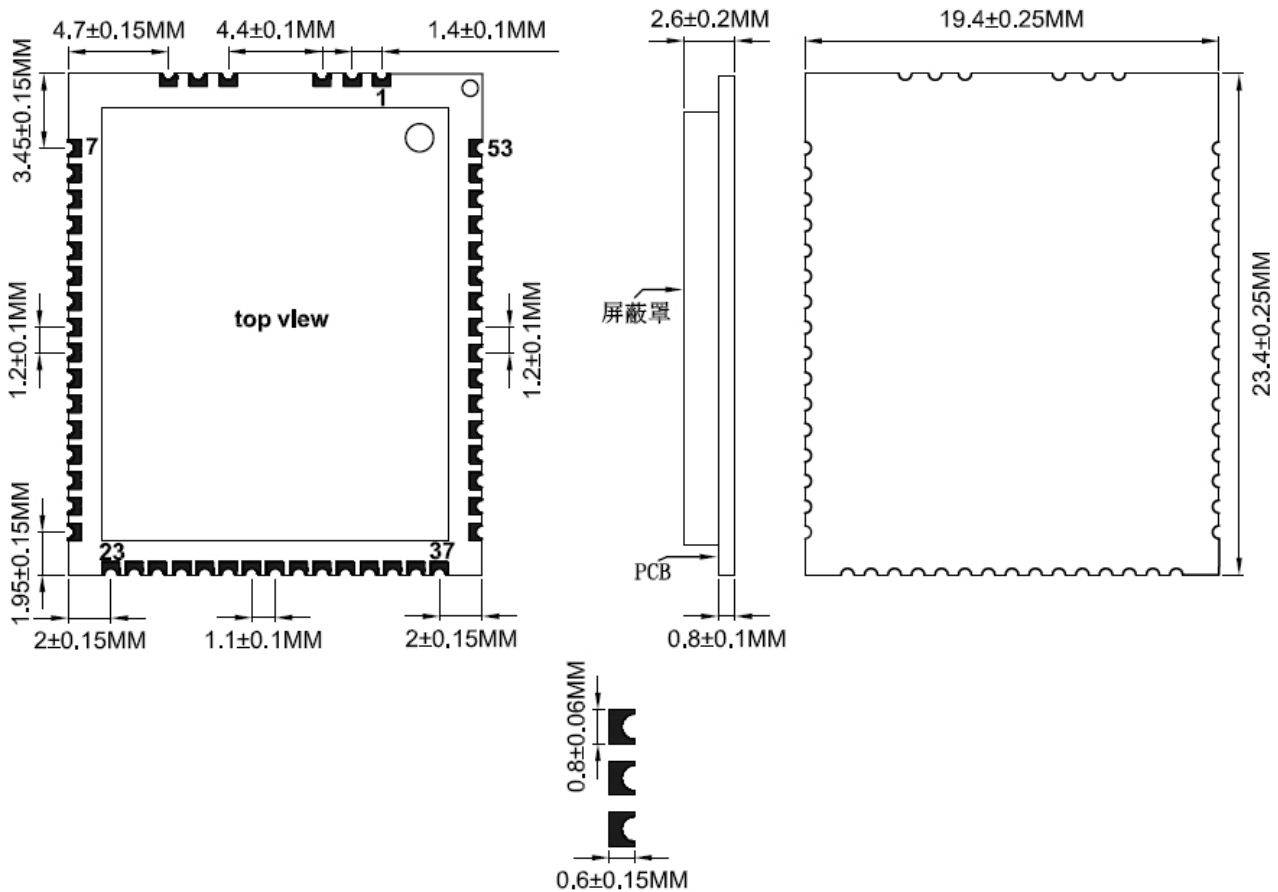


Figure 20: Package dimensions

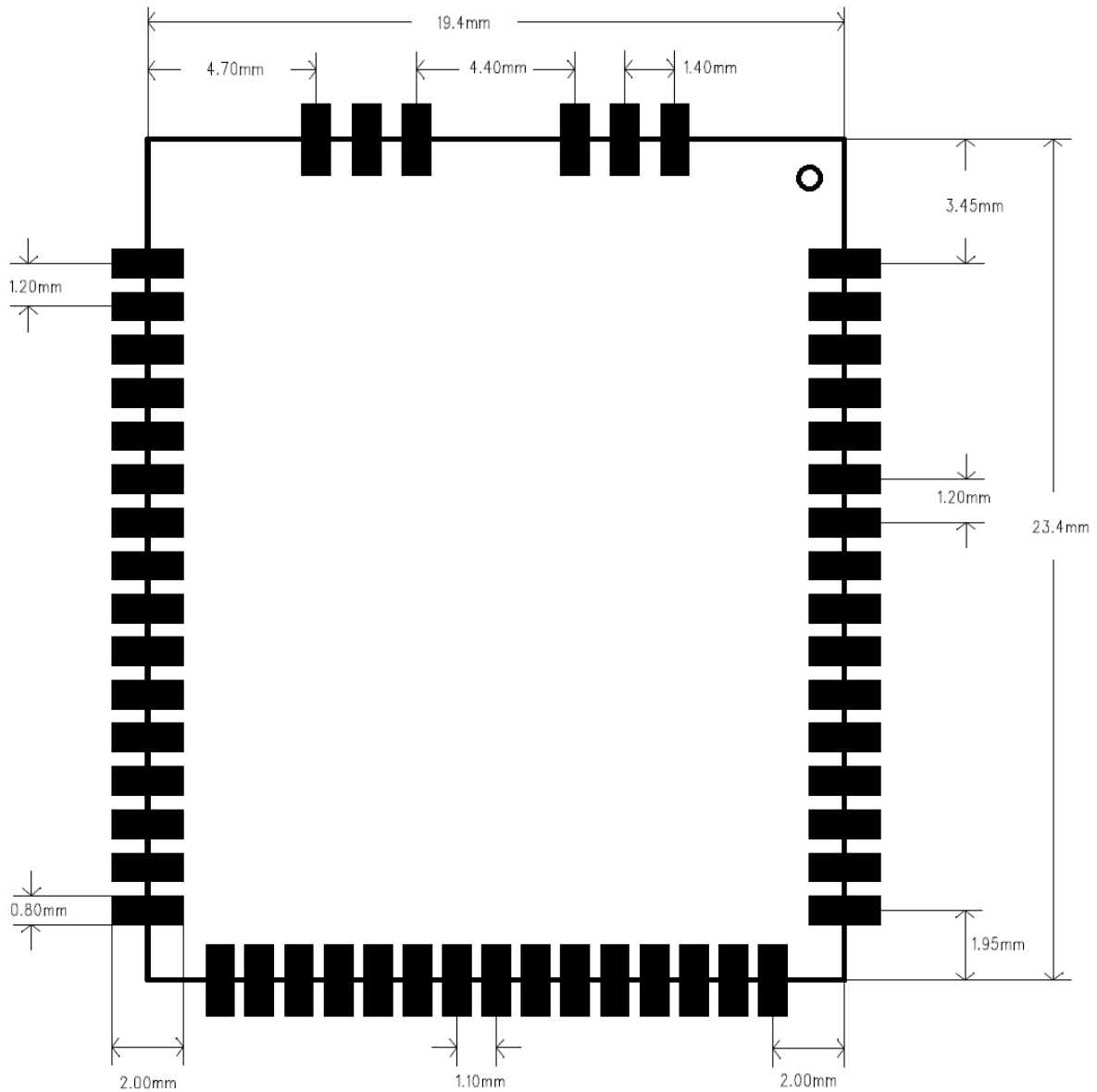


Figure 21: FSC-BW104 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW104 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

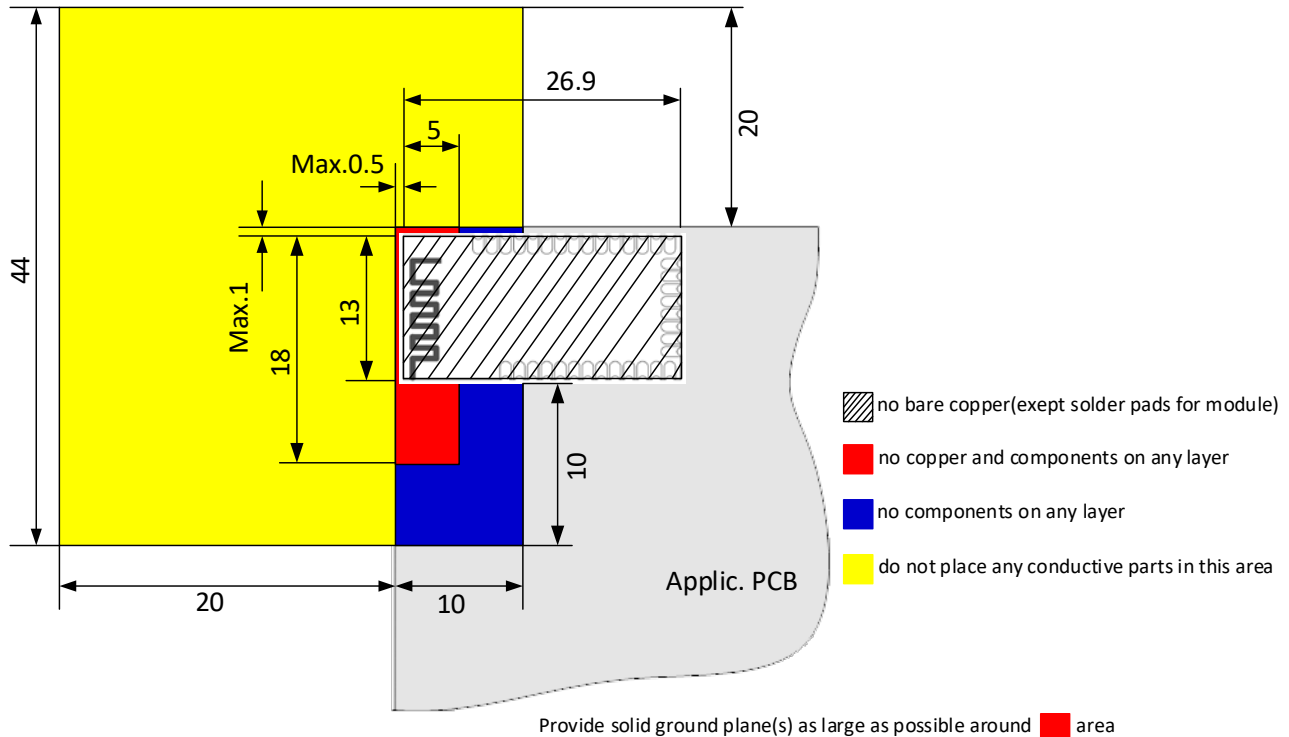


Figure 22: Restricted Area(Reference design) Unit: mm

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

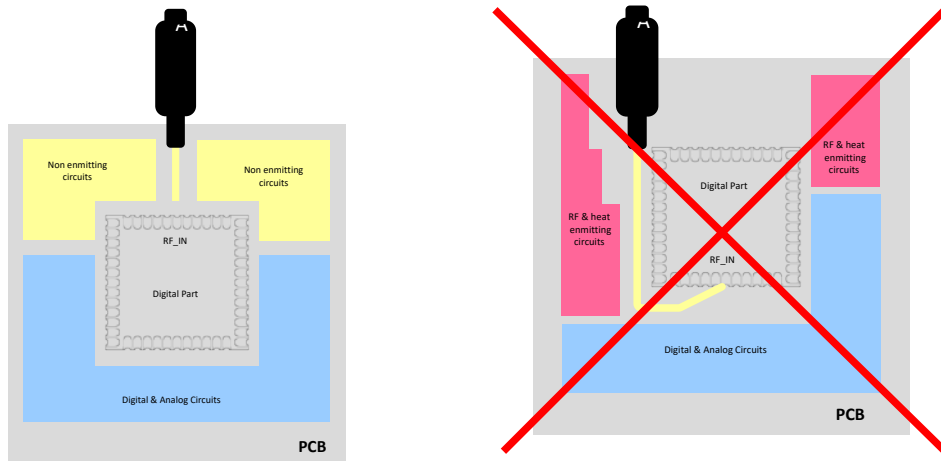


Figure 23: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

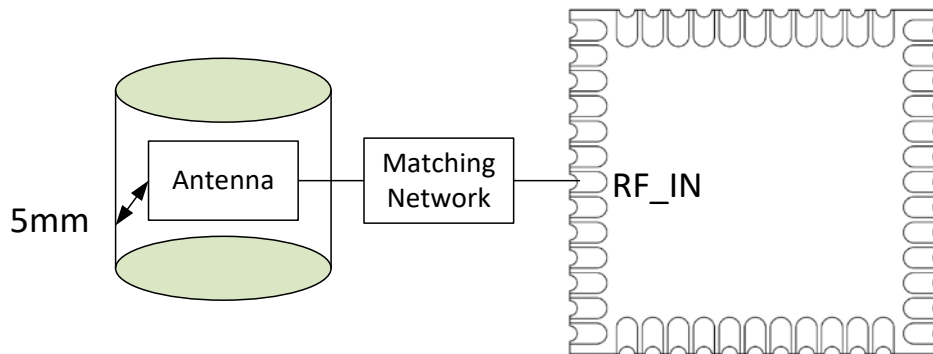


Figure 24: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

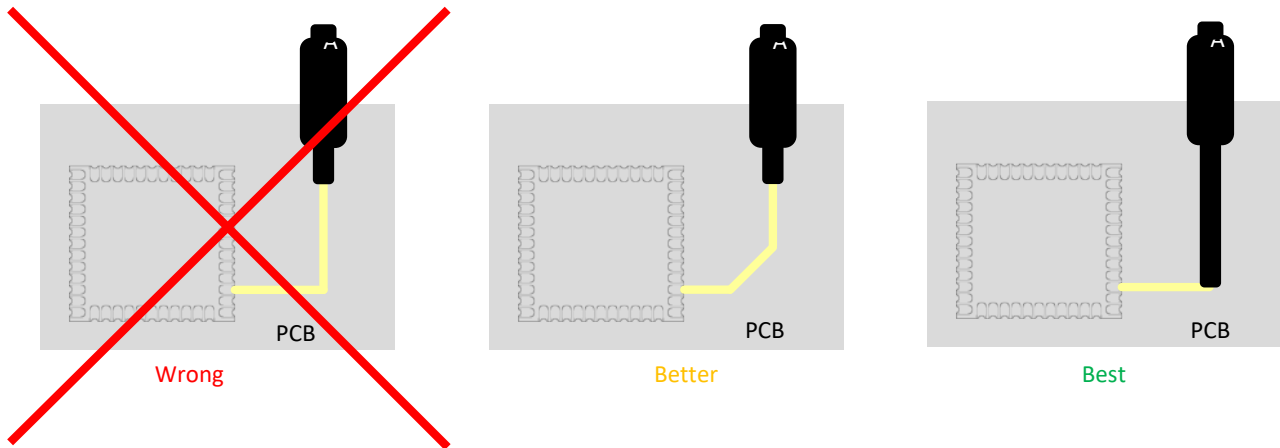


Figure 25: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD

SDIO_CLK

SDIO_DATA_0 ~ SDIO_DATA3

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

BT_UART_RXD

BT_UART_TXD

BT_UART_RTS

BT_UART_CTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

BT_PCM_SYNC

BT_PCM_CLK

BT_PCM_OUT

BT_PCM_IN

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.7 RTC Clock(32.768kHz) Lines Layout Guideline

Follow the same guidelines recommended for the fast clock, It is extremely important that the RTC_CLK trace not be routed next to any digital signals and near the analog audio signals. Furthermore, no digital signals should be routed above or below the RTC_CLK trace to avoid coupling.

9.8 Power Trace Lines Layout Guideline

VBAT Trace Width: $\geq 40\text{mil}$

VIO Trace Width: $\geq 20\text{mil}$

9.9 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW104 Module Ground Pads

Decoupling Capacitors close to FSC-BW104 Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

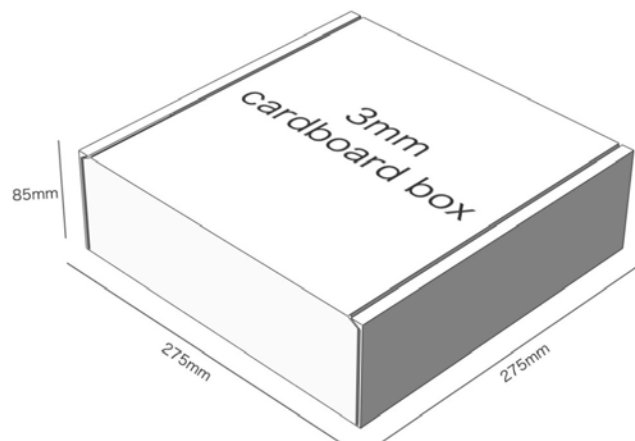
b, Tray Dimension: 140mm * 265mm





Figure 26: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 500PCS Per Carton (Min Carton Package)

Figure 27: Packing Box

11. APPLICATION SCHEMATIC

